Compal Confidential

HCW50 Schematics Document

AMD/Sempron/ATI RX485/SB460 W/s M52/54/56P

2006 / 02 / 28 Rev:0.3 (For PVT)

Security Classification	Compal Secret Data		
Issued Date	2005/05/09	Deciphered Date	2006/03/08

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Project Code: HCW50

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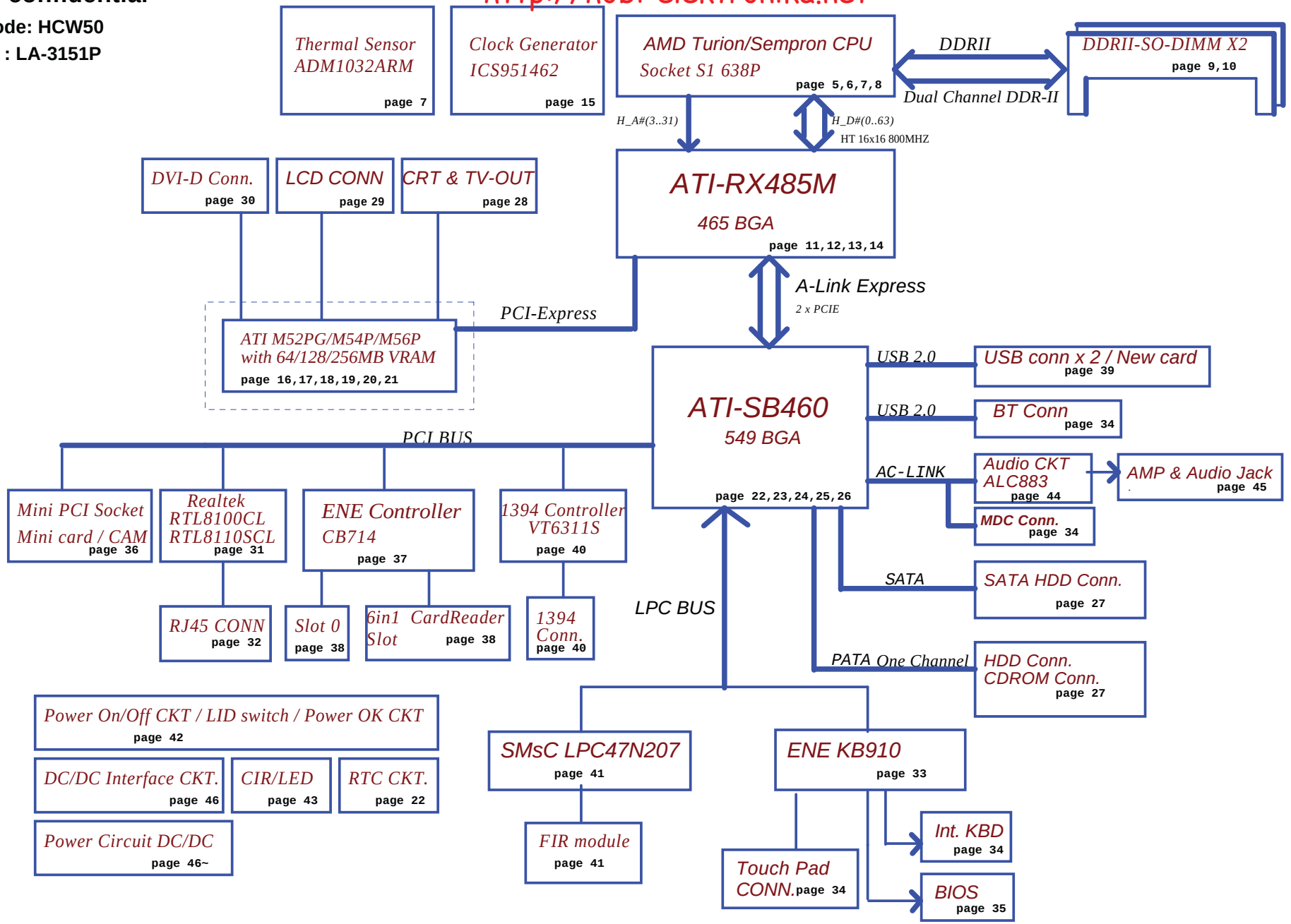

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*
+1.2VS	1.2V switched power rail for PCIE	ON	OFF	OFF
+0.9VS	0.9V switched power rail for VRAM terminator	ON	OFF	OFF
+1.8VALW	1.8V switched power rail	ON	ON	ON*
+VDD_CORE	1.0~1.2V switched power rail for VGA	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
Fintek F75383M	1001 100X b

SB460 SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	
UMA	
UMA's DVI	
LAN(10/100)	
LAN(GIGA)	
MINI CARD1	
MINI CARD2	
SATA-to-IDE	
PATA	
GRAPEVINE	
G72MV Only	
G73 Only	
VRAM	
VRAM 64M	
VRAM 128M	
VRAM 256M	
MEDIA/B	
CIR	
FIR	
GENEVA	
LCM	
Sub-woofer	

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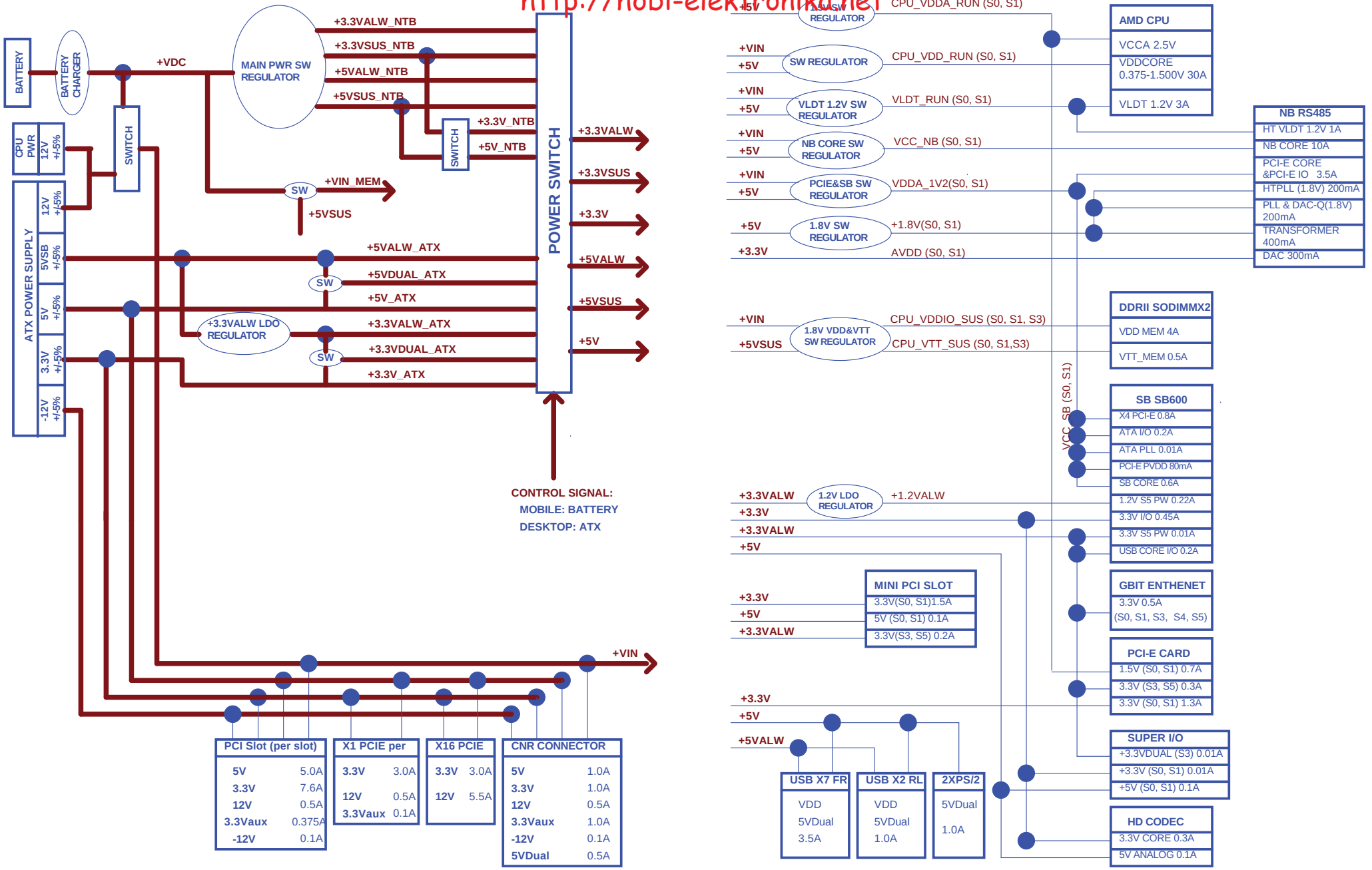

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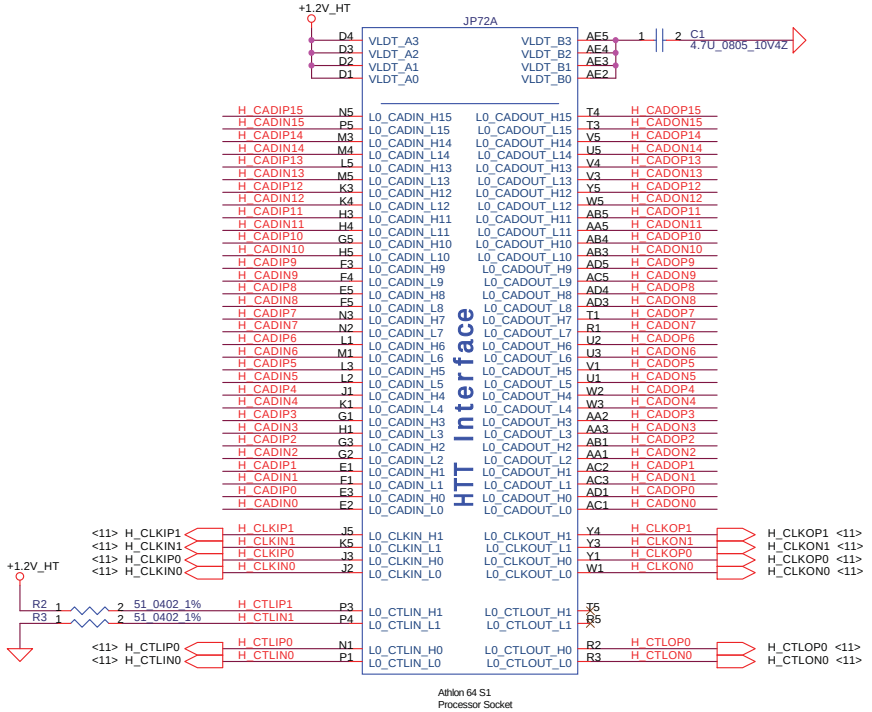
<11> H_CADIP[0..15]
<11> H_CADIN[0..15]
H_CADIP[0..15]
H_CADIN[0..15]

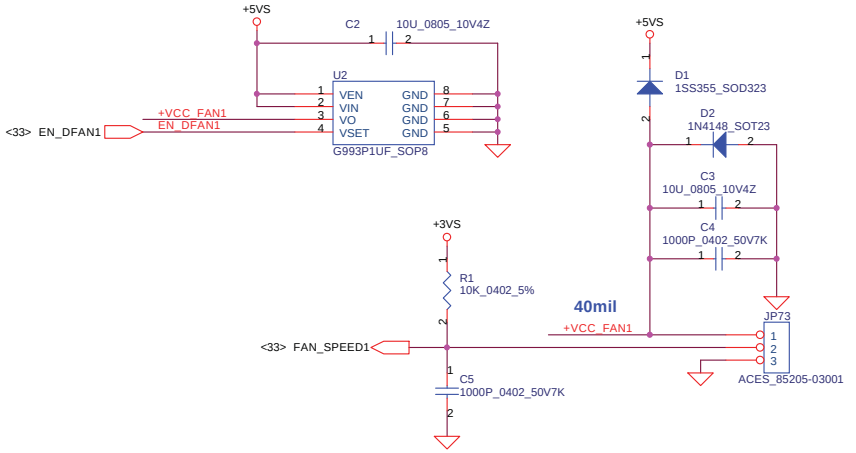
H_CADOP[0..15]
H_CADON[0..15]
H_CADOP[0..15] <11>
H_CADON[0..15] <11>

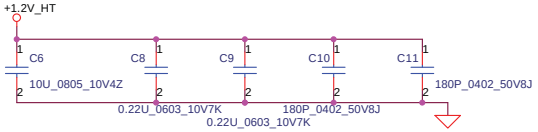
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



FAN1 Conn





LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

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Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

<9> DDR_A_MA[0..15] — DDR_A_MA[0..15]
<10> DDR_B_DQS[0..7] — DDR_B_DQS[0..7]
<10> DDR_B_DQS#[0..7] — DDR_B_DQS#[0..7]

<9> DDR_A_DQS[0..7] — DDR_A_DQS[0..7]
<9> DDR_A_DQS#[0..7] — DDR_A_DQS#[0..7]

+1.8V
R4 39.2_0402_1%~D
R5 39.2_0402_1%~D
PLACE THEM CLOSE TO CPU WITHIN 1"

+0.9VREF_CPU
+0.9V

JP72B

M_VREF W17
VTT_SENSE Y10
M_ZN AE10
M_ZP AF10

DDRII Cmd/Ctrl//Clk

DDR_CS3_DIMMA# V19
DDR_CS2_DIMMA# J22
DDR_CS1_DIMMA# V22
DDR_CS0_DIMMA# T19
DDR_CS3_DIMMB# Y26
DDR_CS2_DIMMB# J24
DDR_CS1_DIMMB# W24
DDR_CS0_DIMMB# U23
DDR_CKE1_DIMMB H26
DDR_CKE0_DIMMB J23
DDR_CKE1_DIMMA J20
DDR_CKE0_DIMMA J21

DDR_A_MA15 K19
DDR_A_MA14 K20
DDR_A_MA13 V24
DDR_A_MA12 K24
DDR_A_MA11 L20
DDR_A_MA10 R19
DDR_A_MA9 L19
DDR_A_MA8 L22
DDR_A_MA7 L21
DDR_A_MA6 M19
DDR_A_MA5 M20
DDR_A_MA4 M24
DDR_A_MA3 M22
DDR_A_MA2 N22
DDR_A_MA1 N21
DDR_A_MA0 R21

DDR_A_BS#2 K22
DDR_A_BS#1 R20
DDR_A_BS#0 T22
DDR_A_RAS# T20
DDR_A_CAS# U20
DDR_A_WE# U21

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

MA0_CLK_H2 Y16 DDR_A_CLK2
MA0_CLK_L2 AA16 DDR_A_CLK#2
MA0_CLK_H1 E16 DDR_A_CLK1
MA0_CLK_L1 E16 DDR_A_CLK#1
MB0_CLK_H2 AF18 DDR_B_CLK2
MB0_CLK_L2 AF17 DDR_B_CLK#2
MB0_CLK_H1 A17 DDR_B_CLK1
MB0_CLK_L1 A18 DDR_B_CLK#1

DDR_A_CLK2 <9>
DDR_A_CLK#2 <9>
DDR_A_CLK1 <9>
DDR_A_CLK#1 <9>
DDR_B_CLK2 <10>
DDR_B_CLK#2 <10>
DDR_B_CLK1 <10>
DDR_B_CLK#1 <10>

MB0_ODT1 W23 DDR_B_ODT1
MB0_ODT0 W26 DDR_B_ODT0
MA0_ODT1 V20 DDR_A_ODT1
MA0_ODT0 U19 DDR_A_ODT0

DDR_B_ODT1 <10>
DDR_B_ODT0 <10>
DDR_A_ODT1 <9>
DDR_A_ODT0 <9>

DDR_B_MA[0..15] <10>

MB_ADD15 J25 DDR_B_MA15
MB_ADD14 J26 DDR_B_MA14
MB_ADD13 W25 DDR_B_MA13
MB_ADD12 L23 DDR_B_MA12
MB_ADD11 L25 DDR_B_MA11
MB_ADD10 U25 DDR_B_MA10
MB_ADD9 L24 DDR_B_MA9
MB_ADD8 M26 DDR_B_MA8
MB_ADD7 L26 DDR_B_MA7
MB_ADD6 N23 DDR_B_MA6
MB_ADD5 N24 DDR_B_MA5
MB_ADD4 N25 DDR_B_MA4
MB_ADD3 N26 DDR_B_MA3
MB_ADD2 P24 DDR_B_MA2
MB_ADD1 P26 DDR_B_MA1
MB_ADD0 T24 DDR_B_MA0

MB_BANK2 K26 DDR_B_BS#2
MB_BANK1 T26 DDR_B_BS#1
MB_BANK0 U26 DDR_B_BS#0

DDR_B_BS#2 <10>
DDR_B_BS#1 <10>
DDR_B_BS#0 <10>

MB_RAS_L U24 DDR_B_RAS#
MB_CAS_L V26 DDR_B_CAS#
MB_WE_L U22 DDR_B_WE#

DDR_B_RAS# <10>
DDR_B_CAS# <10>
DDR_B_WE# <10>

Athlon 64 S1 Processor Socket

DDR_A_CLK2 — C12 1.5P_0402_50V8C — DDR_A_CLK#2
DDR_A_CLK1 — C14 1.5P_0402_50V8C — DDR_A_CLK#1
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

DDR_B_CLK2 — C13 1.5P_0402_50V8C — DDR_B_CLK#2
DDR_B_CLK1 — C15 1.5P_0402_50V8C — DDR_B_CLK#1
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

To reverse SODIMM socket

JP72C

DDRII Data

DDR_B_D63 AD11 MB_DATA63 — MA_DATA63 AA12 DDR_A_D63
DDR_B_D62 AE11 MB_DATA62 — MA_DATA62 AB12 DDR_A_D62
DDR_B_D61 AE14 MB_DATA61 — MA_DATA61 AA14 DDR_A_D61
DDR_B_D60 AE14 MB_DATA60 — MA_DATA60 AB14 DDR_A_D60
DDR_B_D59 Y11 MB_DATA59 — MA_DATA59 W11 DDR_A_D59
DDR_B_D58 AB11 MB_DATA58 — MA_DATA58 Y12 DDR_A_D58
DDR_B_D57 AC12 MB_DATA57 — MA_DATA57 AD13 DDR_A_D57
DDR_B_D56 AF13 MB_DATA56 — MA_DATA56 AB13 DDR_A_D56
DDR_B_D55 AE15 MB_DATA55 — MA_DATA55 AD15 DDR_A_D55
DDR_B_D54 AE16 MB_DATA54 — MA_DATA54 AB15 DDR_A_D54
DDR_B_D53 AC18 MB_DATA53 — MA_DATA53 AB17 DDR_A_D53
DDR_B_D52 AF19 MB_DATA52 — MA_DATA52 Y17 DDR_A_D52
DDR_B_D51 AD14 MB_DATA51 — MA_DATA51 Y14 DDR_A_D51
DDR_B_D50 AC14 MB_DATA50 — MA_DATA50 W14 DDR_A_D50
DDR_B_D49 AE18 MB_DATA49 — MA_DATA49 W16 DDR_A_D49
DDR_B_D48 AD18 MB_DATA48 — MA_DATA48 AD17 DDR_A_D48
DDR_B_D47 AD20 MB_DATA47 — MA_DATA47 Y18 DDR_A_D47
DDR_B_D46 AC20 MB_DATA46 — MA_DATA46 AD19 DDR_A_D46
DDR_B_D45 AF23 MB_DATA45 — MA_DATA45 AD21 DDR_A_D45
DDR_B_D44 AF24 MB_DATA44 — MA_DATA44 AB21 DDR_A_D44
DDR_B_D43 AF20 MB_DATA43 — MA_DATA43 AB18 DDR_A_D43
DDR_B_D42 AE20 MB_DATA42 — MA_DATA42 AA18 DDR_A_D42
DDR_B_D41 AD22 MB_DATA41 — MA_DATA41 AA20 DDR_A_D41
DDR_B_D40 AC22 MB_DATA40 — MA_DATA40 Y20 DDR_A_D40
DDR_B_D39 AF25 MB_DATA39 — MA_DATA39 AA22 DDR_A_D39
DDR_B_D38 AD26 MB_DATA38 — MA_DATA38 Y22 DDR_A_D38
DDR_B_D37 AA25 MB_DATA37 — MA_DATA37 W21 DDR_A_D37
DDR_B_D36 AA26 MB_DATA36 — MA_DATA36 W22 DDR_A_D36
DDR_B_D35 AE24 MB_DATA35 — MA_DATA35 AA21 DDR_A_D35
DDR_B_D34 AD24 MB_DATA34 — MA_DATA34 AB22 DDR_A_D34
DDR_B_D33 AA23 MB_DATA33 — MA_DATA33 AB24 DDR_A_D33
DDR_B_D32 AA24 MB_DATA32 — MA_DATA32 Y24 DDR_A_D32
DDR_B_D31 G24 MB_DATA31 — MA_DATA31 H22 DDR_A_D31
DDR_B_D30 G23 MB_DATA30 — MA_DATA30 H20 DDR_A_D30
DDR_B_D29 D26 MB_DATA29 — MA_DATA29 F22 DDR_A_D29
DDR_B_D28 C26 MB_DATA28 — MA_DATA28 F21 DDR_A_D28
DDR_B_D27 G26 MB_DATA27 — MA_DATA27 J19 DDR_A_D27
DDR_B_D26 G25 MB_DATA26 — MA_DATA26 H24 DDR_A_D26
DDR_B_D25 E24 MB_DATA25 — MA_DATA25 F22 DDR_A_D25
DDR_B_D24 E23 MB_DATA24 — MA_DATA24 F20 DDR_A_D24
DDR_B_D23 C24 MB_DATA23 — MA_DATA23 C23 DDR_A_D23
DDR_B_D22 B24 MB_DATA22 — MA_DATA22 B22 DDR_A_D22
DDR_B_D21 C20 MB_DATA21 — MA_DATA21 F18 DDR_A_D21
DDR_B_D20 B20 MB_DATA20 — MA_DATA20 E18 DDR_A_D20
DDR_B_D19 C25 MB_DATA19 — MA_DATA19 F20 DDR_A_D19
DDR_B_D18 D24 MB_DATA18 — MA_DATA18 D22 DDR_A_D18
DDR_B_D17 A21 MB_DATA17 — MA_DATA17 C19 DDR_A_D17
DDR_B_D16 D20 MB_DATA16 — MA_DATA16 G18 DDR_A_D16
DDR_B_D15 D18 MB_DATA15 — MA_DATA15 G17 DDR_A_D15
DDR_B_D14 C18 MB_DATA14 — MA_DATA14 C17 DDR_A_D14
DDR_B_D13 D14 MB_DATA13 — MA_DATA13 F14 DDR_A_D13
DDR_B_D12 C14 MB_DATA12 — MA_DATA12 E14 DDR_A_D12
DDR_B_D11 A20 MB_DATA11 — MA_DATA11 H17 DDR_A_D11
DDR_B_D10 A19 MB_DATA10 — MA_DATA10 E17 DDR_A_D10
DDR_B_D9 A16 MB_DATA9 — MA_DATA9 E15 DDR_A_D9
DDR_B_D8 A15 MB_DATA8 — MA_DATA8 H15 DDR_A_D8
DDR_B_D7 A13 MB_DATA7 — MA_DATA7 E13 DDR_A_D7
DDR_B_D6 D12 MB_DATA6 — MA_DATA6 C13 DDR_A_D6
DDR_B_D5 E11 MB_DATA5 — MA_DATA5 H12 DDR_A_D5
DDR_B_D4 G11 MB_DATA4 — MA_DATA4 H11 DDR_A_D4
DDR_B_D3 B14 MB_DATA3 — MA_DATA3 G14 DDR_A_D3
DDR_B_D2 A14 MB_DATA2 — MA_DATA2 H14 DDR_A_D2
DDR_B_D1 A11 MB_DATA1 — MA_DATA1 F12 DDR_A_D1
DDR_B_D0 C11 MB_DATA0 — MA_DATA0 G12 DDR_A_D0

<10> DDR_B_D[0..63]
DDR_A_D[0..63] <9>

DDR_B_DM7 AD12 MB_DM7 — MA_DM7 Y13 DDR_A_DM7
DDR_B_DM6 AC16 MB_DM6 — MA_DM6 AB16 DDR_A_DM6
DDR_B_DM5 AE22 MB_DM5 — MA_DM5 Y19 DDR_A_DM5
DDR_B_DM4 AB26 MB_DM4 — MA_DM4 AC24 DDR_A_DM4
DDR_B_DM3 E25 MB_DM3 — MA_DM3 F24 DDR_A_DM3
DDR_B_DM2 A22 MB_DM2 — MA_DM2 E19 DDR_A_DM2
DDR_B_DM1 B16 MB_DM1 — MA_DM1 C15 DDR_A_DM1
DDR_B_DM0 A12 MB_DM0 — MA_DM0 E12 DDR_A_DM0

<10> DDR_B_DM[0..7]
DDR_A_DM[0..7] <9>

DDR_B_DQS7 AE12 MB_DQS_H7 — MA_DQS_H7 W12 DDR_A_DQS7
DDR_B_DQS#7 AE12 MB_DQS_L7 — MA_DQS_L7 W13 DDR_A_DQS#7
DDR_B_DQS6 AE16 MB_DQS_H6 — MA_DQS_H6 Y15 DDR_A_DQS6
DDR_B_DQS#6 AD16 MB_DQS_L6 — MA_DQS_L6 W15 DDR_A_DQS#6
DDR_B_DQS5 AF21 MB_DQS_H5 — MA_DQS_H5 AB19 DDR_A_DQS5
DDR_B_DQS#5 AF22 MB_DQS_L5 — MA_DQS_L5 AB20 DDR_A_DQS#5
DDR_B_DQS4 AC25 MB_DQS_H4 — MA_DQS_H4 AD23 DDR_A_DQS4
DDR_B_DQS#4 AC26 MB_DQS_L4 — MA_DQS_L4 AC23 DDR_A_DQS#4
DDR_B_DQS3 F26 MB_DQS_H3 — MA_DQS_H3 G22 DDR_A_DQS3
DDR_B_DQS#3 E26 MB_DQS_L3 — MA_DQS_L3 G21 DDR_A_DQS#3
DDR_B_DQS2 A24 MB_DQS_H2 — MA_DQS_H2 C22 DDR_A_DQS2
DDR_B_DQS#2 A23 MB_DQS_L2 — MA_DQS_L2 C21 DDR_A_DQS#2
DDR_B_DQS1 D16 MB_DQS_H1 — MA_DQS_H1 G16 DDR_A_DQS1
DDR_B_DQS#1 C16 MB_DQS_L1 — MA_DQS_L1 G15 DDR_A_DQS#1
DDR_B_DQS0 C12 MB_DQS_H0 — MA_DQS_H0 G13 DDR_A_DQS0
DDR_B_DQS#0 B12 MB_DQS_L0 — MA_DQS_L0 H13 DDR_A_DQS#0

DDR: DATA
Athlon 64 S1 Processor Socket

To normal SODIMM socket

ATI check ,Use +0.9V PWR , can delete or not

+1.8V
R6 1K_0402_1%
R7 1K_0402_1%
+0.9VREF_CPU
C16 1000P_0402_50V7K
C18 0.1U_0402_16V4Z
C19 1000P_0402_50V7K
C20 1U_0402_6.3V4Z
VDD_VREF_SUS_CPU
LAYOUT:PLACE CLOSE TO CPU

A1 A26
Athlon 64 S1g1
uPGA638
Top View
AF1

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ATI-ONI Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

50mil width(600mA)

SB460 ONLY

place them to CPU within 1"

Modify 11/22

HDT Connector

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

SMBus Address: 1001110X (b)

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

Place within 0.5" from CPU 25mil/6mil/6mil/6mil/25mil

AMD NPT S1 SOCKET Processor Socket

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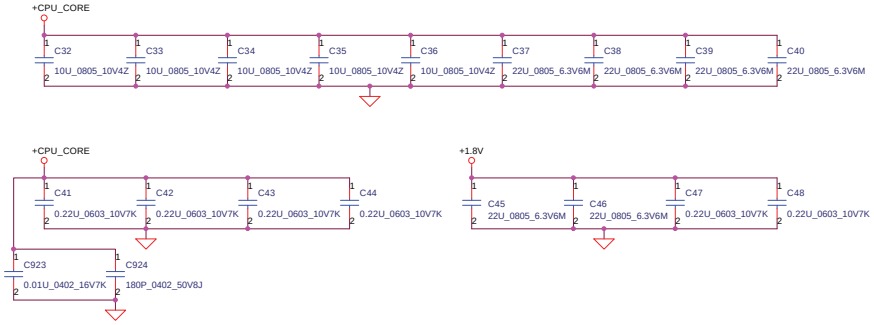
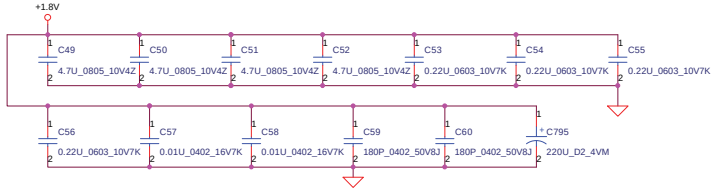
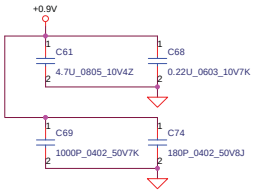
BOTTOMSIDE DECOUPLING



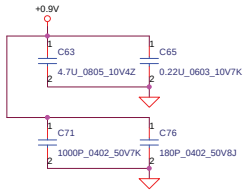
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

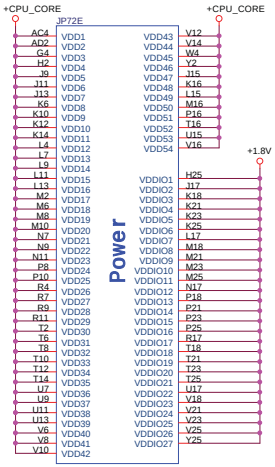


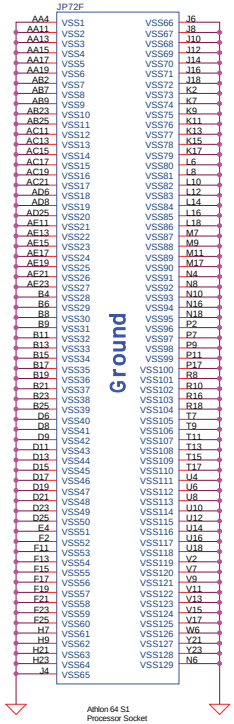
CPU left-hand side

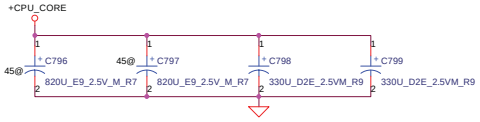


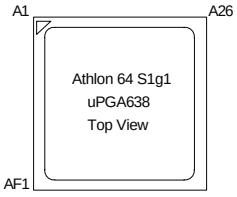
CPU right-hand side











PROCESSOR POWER AND GROUND

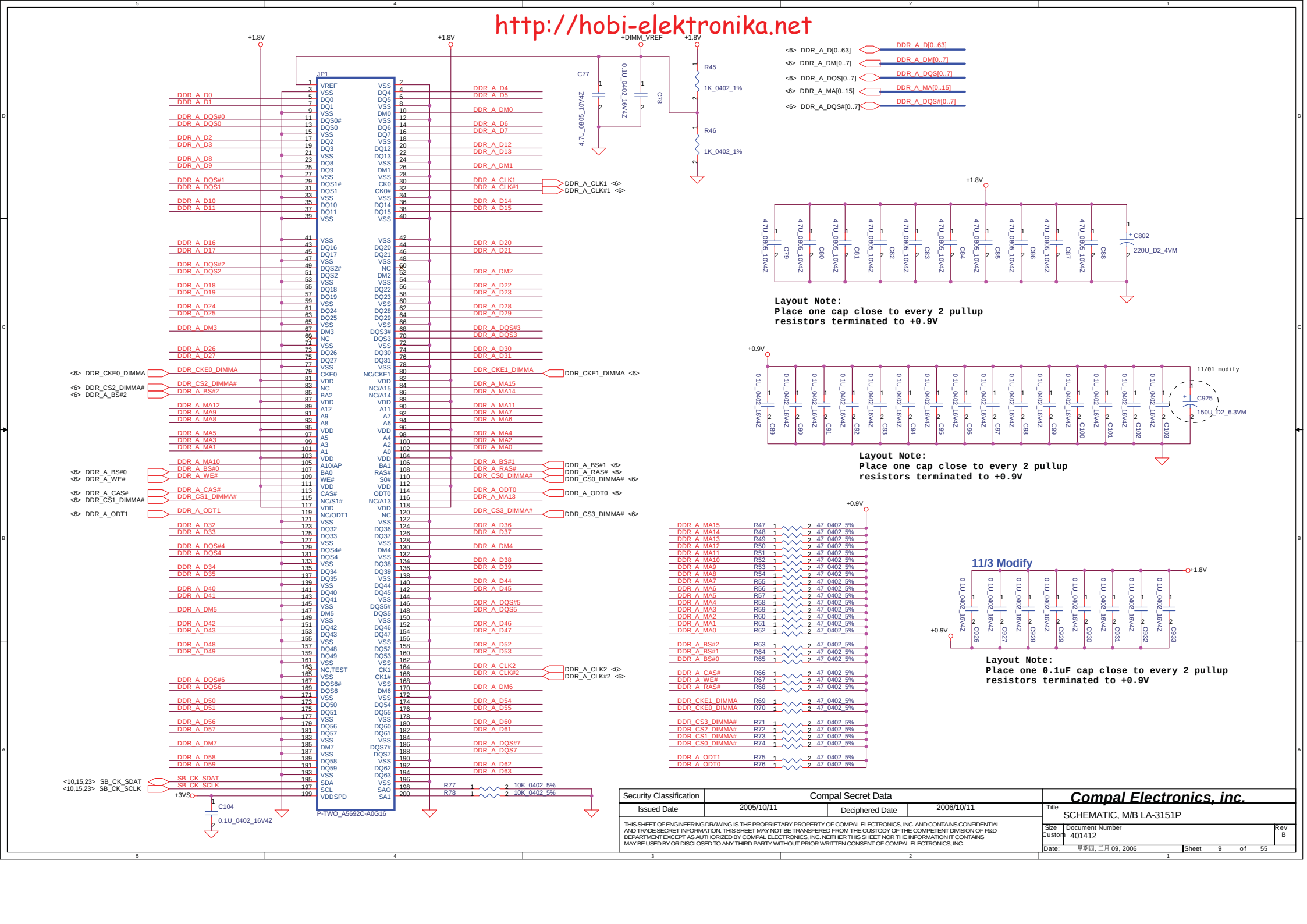
Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

Size: C | Document Number: 401412 | Rev: B

Date: 星期四, 三月 09, 2006 | Sheet 8 of 55



Security Classification	Compal Secret Data		
Issued Date	2005/10/11	Deciphered Date	2006/10/11

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

Size	Document Number	Rev
Custom	401412	B

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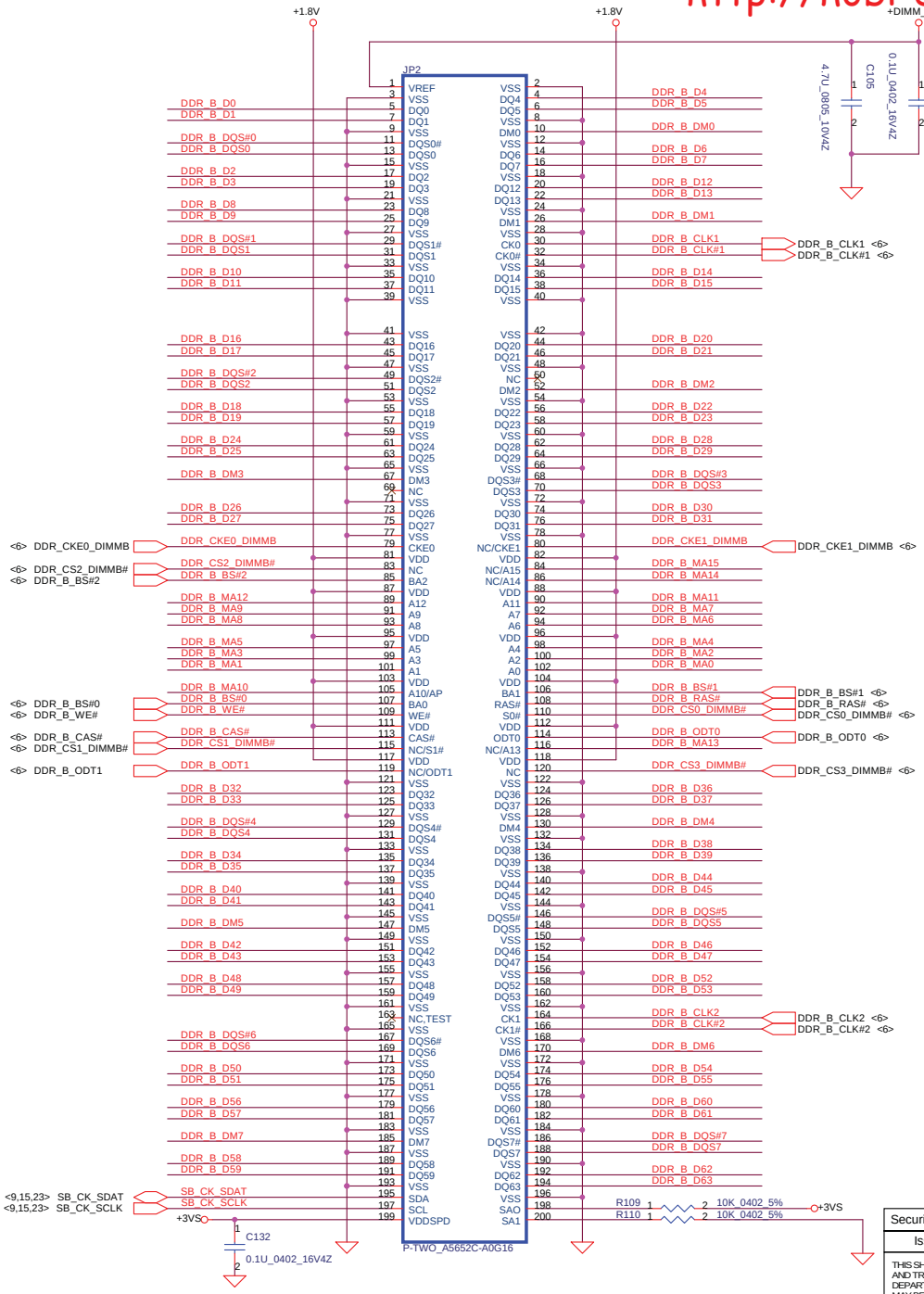
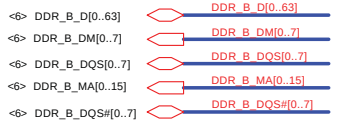
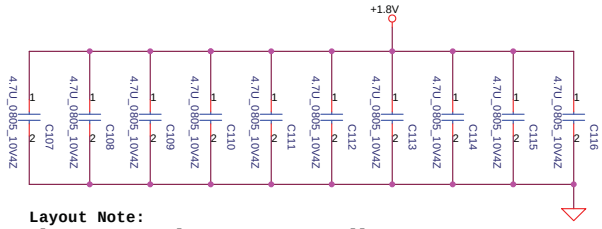
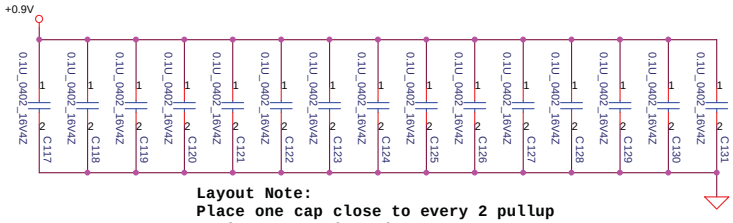


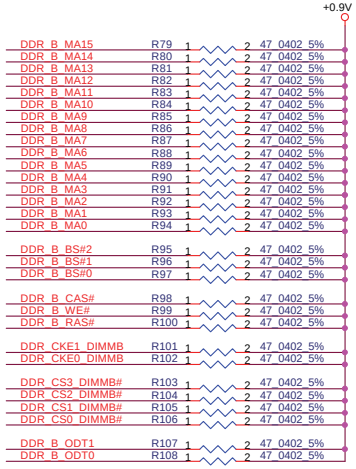




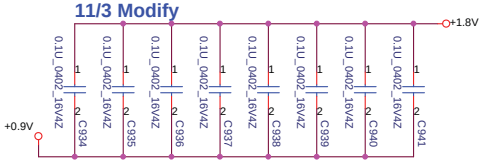
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



11/3 Modify



Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

Security Classification	Compal Secret Data		
Issued Date	2005/10/11	Deciphered Date	2006/10/11

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

Size	Document Number	Rev
Custom	401412	B

Date: 星期四, 三月 09, 2006 Sheet 10 of 55

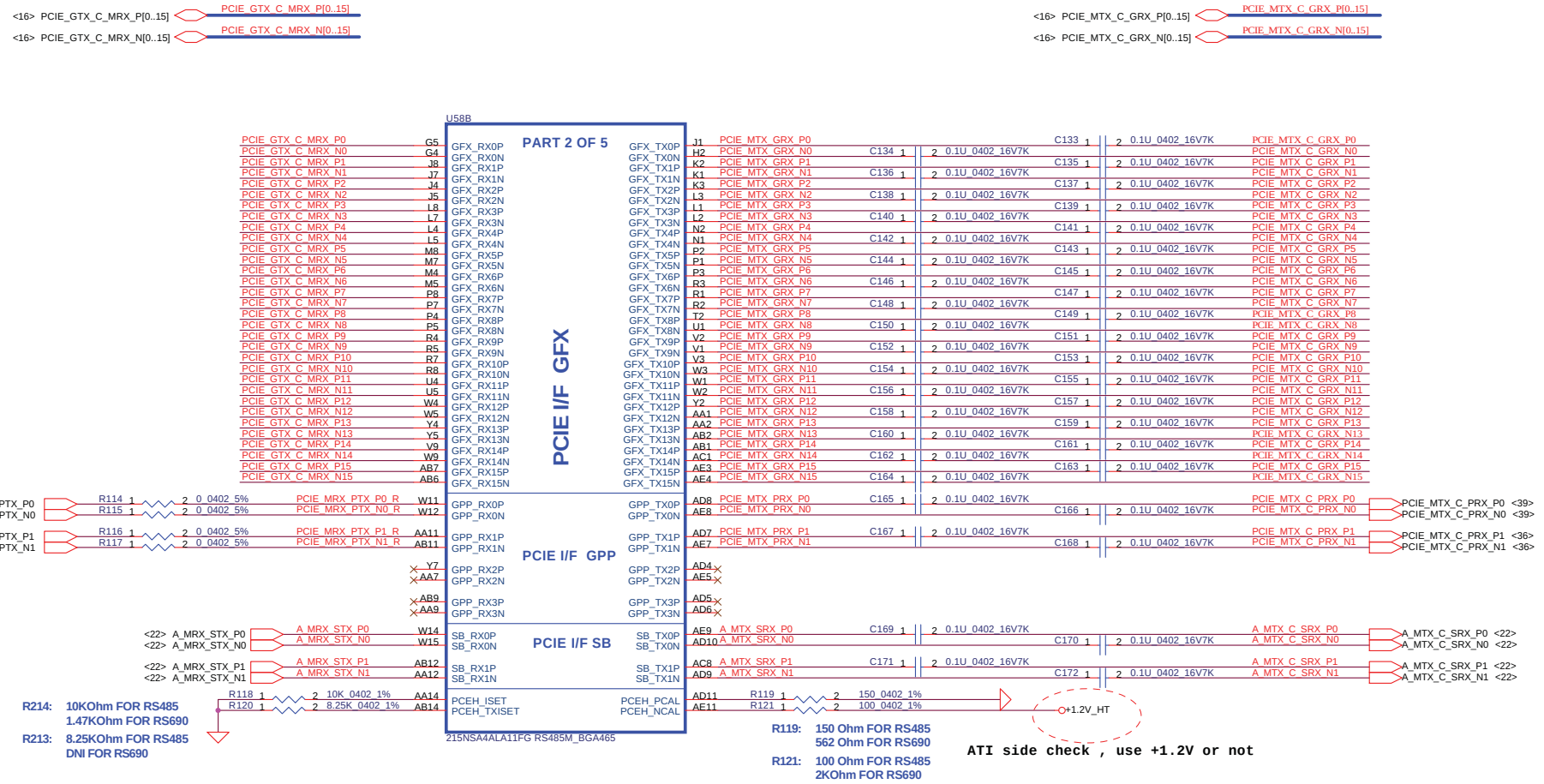
Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

Size	Document Number	Rev
Custom	401412	B

Date: 星期四, 三月 09, 2006 Sheet 11 of 55



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Size	Document Number	Rev
Custom	401412	B

Date: 星期四, 三月 09, 2006 Sheet 12 of 55

ATI check , CRT / TV/ LVDS can delete or not when I use RX485

Modify 11/29

Modify : 11/07

Modify 11/29

LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

U58C — PART 3 OF 5 — 215NSA4ALA11FG RS485M_BGA465

Security Classification	Compal Secret Data
Issued Date	2005/03/08
Deciphered Date	2006/03/08

Compal Electronics, inc.

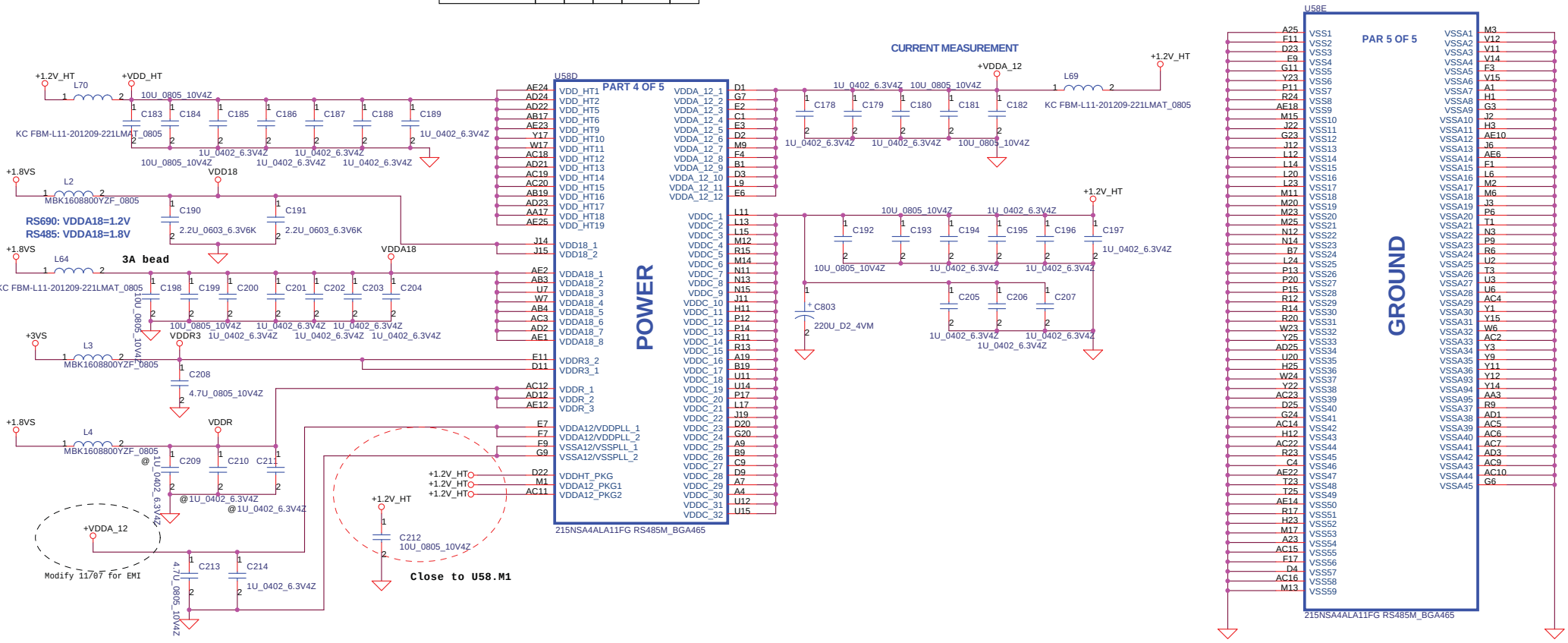
Title: SCHEMATIC, M/B LA-3151P

Size: Custom | Document Number: 401412 | Rev: B

Date: 星期四, 三月 09, 2006 | Sheet 13 of 55

NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



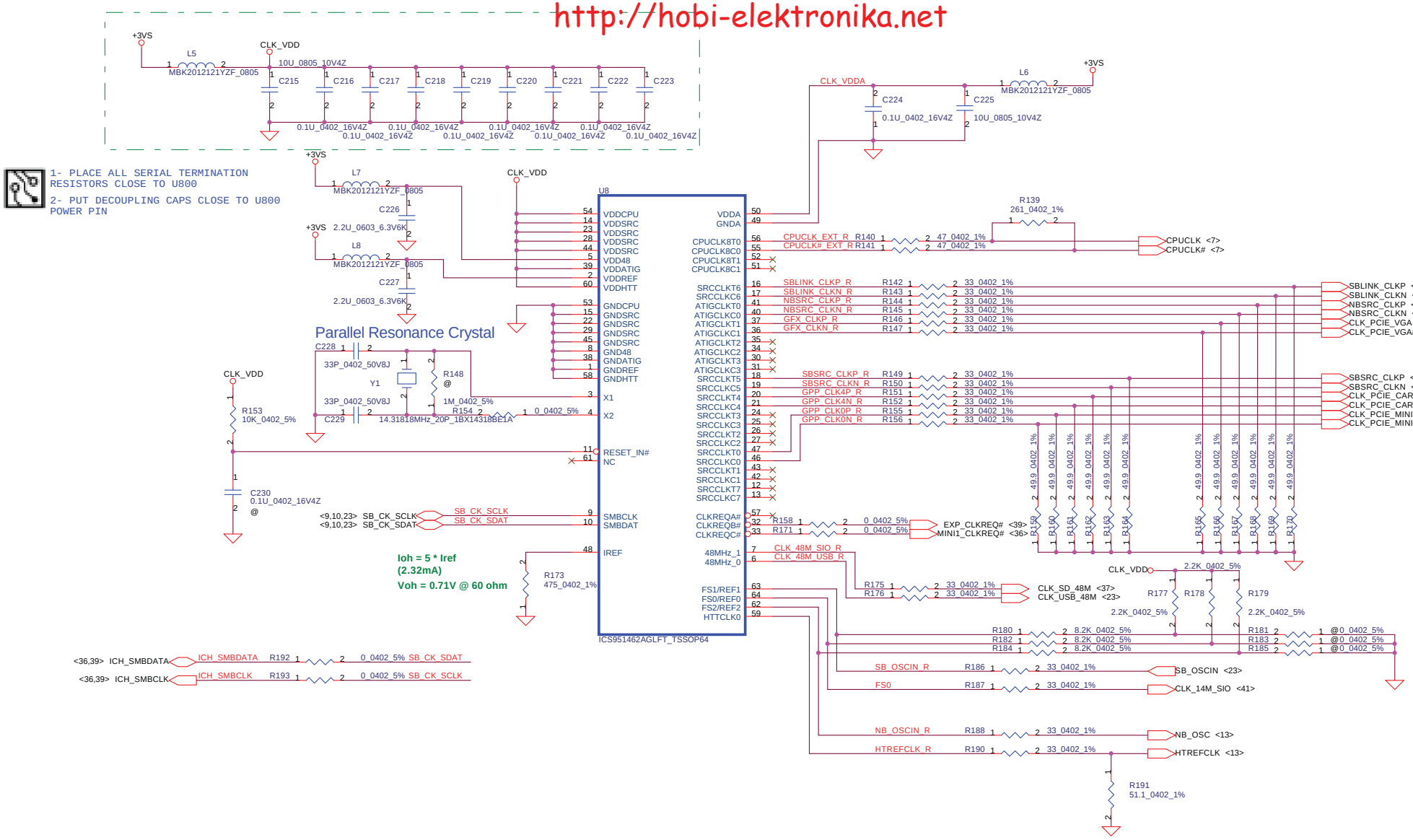
Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

Size: Custom | Document Number: 401412 | Rev: B

Date: 星期四, 三月 09, 2006 | Sheet 14 of 55



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

Size: Custom | Document Number: 401412 | Rev: B

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PCIE Lane Reversal

<15> CLK_PCIE_VGA → CLK_PCIE_VGA AL28
<15> CLK_PCIE_VGA# → CLK_PCIE_VGA# AK28

PCIE_GTX_C_MRX_N15	C233	0.1U_0402_16V7K	PCIE_GTX_MRX_N15	AK27
PCIE_GTX_C_MRX_P15	C233	0.1U_0402_16V7K	PCIE_GTX_MRX_P15	AJ27
PCIE_GTX_C_MRX_N14	C234	0.1U_0402_16V7K	PCIE_GTX_MRX_N14	AJ25
PCIE_GTX_C_MRX_P14	C234	0.1U_0402_16V7K	PCIE_GTX_MRX_P14	AH25
PCIE_GTX_C_MRX_N13	C236	0.1U_0402_16V7K	PCIE_GTX_MRX_N13	AH28
PCIE_GTX_C_MRX_P13	C235	0.1U_0402_16V7K	PCIE_GTX_MRX_P13	AG28
PCIE_GTX_C_MRX_N12	C238	0.1U_0402_16V7K	PCIE_GTX_MRX_N12	AG27
PCIE_GTX_C_MRX_P12	C237	0.1U_0402_16V7K	PCIE_GTX_MRX_P12	AF27
PCIE_GTX_C_MRX_N11	C240	0.1U_0402_16V7K	PCIE_GTX_MRX_N11	AF25
PCIE_GTX_C_MRX_P11	C239	0.1U_0402_16V7K	PCIE_GTX_MRX_P11	AE25
PCIE_GTX_C_MRX_N10	C242	0.1U_0402_16V7K	PCIE_GTX_MRX_N10	AE28
PCIE_GTX_C_MRX_P10	C241	0.1U_0402_16V7K	PCIE_GTX_MRX_P10	AD28
PCIE_GTX_C_MRX_N9	C244	0.1U_0402_16V7K	PCIE_GTX_MRX_N9	AD27
PCIE_GTX_C_MRX_P9	C243	0.1U_0402_16V7K	PCIE_GTX_MRX_P9	AC27
PCIE_GTX_C_MRX_N8	C246	0.1U_0402_16V7K	PCIE_GTX_MRX_N8	AC25
PCIE_GTX_C_MRX_P8	C245	0.1U_0402_16V7K	PCIE_GTX_MRX_P8	AB25
PCIE_GTX_C_MRX_N7	C248	0.1U_0402_16V7K	PCIE_GTX_MRX_N7	AB28
PCIE_GTX_C_MRX_P7	C247	0.1U_0402_16V7K	PCIE_GTX_MRX_P7	AA28
PCIE_GTX_C_MRX_N6	C251	0.1U_0402_16V7K	PCIE_GTX_MRX_N6	AA27
PCIE_GTX_C_MRX_P6	C249	0.1U_0402_16V7K	PCIE_GTX_MRX_P6	Y27
PCIE_GTX_C_MRX_N5	C253	0.1U_0402_16V7K	PCIE_GTX_MRX_N5	Y25
PCIE_GTX_C_MRX_P5	C254	0.1U_0402_16V7K	PCIE_GTX_MRX_P5	W25
PCIE_GTX_C_MRX_N4	C255	0.1U_0402_16V7K	PCIE_GTX_MRX_N4	W28
PCIE_GTX_C_MRX_P4	C254	0.1U_0402_16V7K	PCIE_GTX_MRX_P4	V28
PCIE_GTX_C_MRX_N3	C257	0.1U_0402_16V7K	PCIE_GTX_MRX_N3	V27
PCIE_GTX_C_MRX_P3	C256	0.1U_0402_16V7K	PCIE_GTX_MRX_P3	U27
PCIE_GTX_C_MRX_N2	C259	0.1U_0402_16V7K	PCIE_GTX_MRX_N2	U25
PCIE_GTX_C_MRX_P2	C258	0.1U_0402_16V7K	PCIE_GTX_MRX_P2	T25
PCIE_GTX_C_MRX_N1	C261	0.1U_0402_16V7K	PCIE_GTX_MRX_N1	T28
PCIE_GTX_C_MRX_P1	C260	0.1U_0402_16V7K	PCIE_GTX_MRX_P1	R28
PCIE_GTX_C_MRX_N0	C263	0.1U_0402_16V7K	PCIE_GTX_MRX_N0	R27
PCIE_GTX_C_MRX_P0	C264	0.1U_0402_16V7K	PCIE_GTX_MRX_P0	P27

PCIE_MTX_C_GRX_N15	AJ31	PCIE_MTX_C_GRX_N7	AA32
PCIE_MTX_C_GRX_P15	AH31	PCIE_MTX_C_GRX_P7	Y32
PCIE_MTX_C_GRX_N14	AH30	PCIE_MTX_C_GRX_N6	Y31
PCIE_MTX_C_GRX_P14	AG30	PCIE_MTX_C_GRX_P6	W31
PCIE_MTX_C_GRX_N13	AG32	PCIE_MTX_C_GRX_N5	W30
PCIE_MTX_C_GRX_P13	AF32	PCIE_MTX_C_GRX_P5	V30
PCIE_MTX_C_GRX_N12	AF31	PCIE_MTX_C_GRX_N4	V32
PCIE_MTX_C_GRX_P12	AE31	PCIE_MTX_C_GRX_P4	U32
PCIE_MTX_C_GRX_N11	AE30	PCIE_MTX_C_GRX_N3	U31
PCIE_MTX_C_GRX_P11	AD30	PCIE_MTX_C_GRX_P3	T31
PCIE_MTX_C_GRX_N10	AD32	PCIE_MTX_C_GRX_N2	T30
PCIE_MTX_C_GRX_P10	AC32	PCIE_MTX_C_GRX_P2	R30
PCIE_MTX_C_GRX_N9	AC31	PCIE_MTX_C_GRX_N1	R32
PCIE_MTX_C_GRX_P9	AB31	PCIE_MTX_C_GRX_P1	P32
PCIE_MTX_C_GRX_N8	AB30	PCIE_MTX_C_GRX_N0	P31
PCIE_MTX_C_GRX_P8	AA30	PCIE_MTX_C_GRX_P0	N31

<12> PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]
<12> PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]
<12> PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]
<12> PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]

Thermal sensor

+3VS
R210 2.2K_0402_5% THM@
U10: VDD, D+, D-, OVERT#, SCLK, SDATA, ALERT#, GND
THERM_SCL, THERM_SDA, THER_ALERT#
R211 2.2K_0402_5% THM@
R212 0_0402_5% THM@
C264 THM@ 2200P_0402_50V7K
THM@ MAX6649MUA_8UMAX

Spread spectrum

U11: ASM3P1819N-SR_SO8 SSC@
VDD, REF, XIN MODOUT, XOUT NC, VSS PD#
R222 SSC@ 0_0603_5%
R226 22_0402_5% SSC@ OSC_SPREAD
C265 SSC@ 0.1U_0402_16V4Z
C266 0.1U_0402_16V4Z
X1 27MHZ_15P
R230 1K_0402_5%
OSC_IN
Memory Interface SS
Minimize distance from X1 pin3 to U3 pin1
Keep away from other signal at last 25mils

+1.2VS
R215 2K_0402_1% AE24
R217 562_0603_1% AD24
R218 1.47K_0603_1% AB24
<13,22,27,33,36,41> NB_RST# → R220 0_0402_5% AG24
R221 10K_0402_5% AA24 AF24
PCIE_TEST
PERST#_MASK
R224 4.7K_0402_5% THERM_SDA AE12
R225 4.7K_0402_5% THERM_SCL AE12
D+ AG12
D- AH12
OSC_IN R227 121_0402_1% AL26
R229 71.5_0402_1% AM26
M56P
M56@

PCI EXPRESS

PCIE_REFCLKP, PCIE_REFCLKN
PCIE_TX0P, PCIE_TX0N, PCIE_TX1P, PCIE_TX1N, PCIE_TX2P, PCIE_TX2N, PCIE_TX3P, PCIE_TX3N, PCIE_TX4P, PCIE_TX4N, PCIE_TX5P, PCIE_TX5N, PCIE_TX6P, PCIE_TX6N, PCIE_TX7P, PCIE_TX7N, PCIE_TX8P, PCIE_TX8N, PCIE_TX9P, PCIE_TX9N, PCIE_TX10P, PCIE_TX10N, PCIE_TX11P, PCIE_TX11N, PCIE_TX12P, PCIE_TX12N, PCIE_TX13P, PCIE_TX13N, PCIE_TX14P, PCIE_TX14N, PCIE_TX15P, PCIE_TX15N
PCIE_RX0P, PCIE_RX0N, PCIE_RX1P, PCIE_RX1N, PCIE_RX2P, PCIE_RX2N, PCIE_RX3P, PCIE_RX3N, PCIE_RX4P, PCIE_RX4N, PCIE_RX5P, PCIE_RX5N, PCIE_RX6P, PCIE_RX6N, PCIE_RX7P, PCIE_RX7N, PCIE_RX8P, PCIE_RX8N, PCIE_RX9P, PCIE_RX9N, PCIE_RX10P, PCIE_RX10N, PCIE_RX11P, PCIE_RX11N, PCIE_RX12P, PCIE_RX12N, PCIE_RX13P, PCIE_RX13N, PCIE_RX14P, PCIE_RX14N, PCIE_RX15P, PCIE_RX15N
PCIE_CALRN, PCIE_CALRP, PCIE_CALI

THERMAL

DPLUS, DMINUS, DDC3DATA, DDC3CLK

XTAL

XTALIN, XTALOUT

GPIO

GPIO_0	AD4	R194	10K_0402_5%
GPIO_1	AD2	R195	10K_0402_5%
GPIO_2	AD1		
GPIO_3	AD3		
GPIO_4	AC1	R196	2@10K_0402_5%
GPIO_5	AC2	R197	10K_0402_5%
GPIO_6	AC3		
GPIO_7_BLON	AB2	R198	2@10K_0402_5%
GPIO_8	AC6		
GPIO_9	AC5	R199	@ 10K_0402_5%
GPIO_10	AC4	TP1	
GPIO_11	AB3	R200	@ 10K_0402_5%
GPIO_12	AB4	R201	X76@ 10K_0402_5%
GPIO_13	AB5	R202	X76@ 10K_0402_5%
GPIO_14	AD5		
GPIO_15	AB8	POWER_SEL	POWER_SEL <53>
GPIO_16	AA8	OSC_SPREAD	
GPIO_17	AB7	THER_ALERT#	
NC	AB6		
VREFG	AC8	R203 499_0402_1%	
		R204 499_0402_1%	
		C250 0.1U_0402_16V4Z	

Low -> VDDC=1.2V
High -> VDDC=1.0V

VIP HOST/ EXTERNAL TMDS

NC_DVOVMODE_0, NC_DVOVMODE_1
DVPCNTL_0, DVPCNTL_1, DVPCNTL_2, DVPCLK
DVPDATA_0, DVPDATA_1, DVPDATA_2, DVPDATA_3, DVPDATA_4, DVPDATA_5, DVPDATA_6, DVPDATA_7, DVPDATA_8, DVPDATA_9, DVPDATA_10, DVPDATA_11, DVPDATA_12, DVPDATA_13, DVPDATA_14, DVPDATA_15, DVPDATA_16, DVPDATA_17, DVPDATA_18, DVPDATA_19, DVPDATA_20, DVPDATA_21, DVPDATA_22, DVPDATA_23

TP2, TP3, TP4
R205 4.7K_0402_5%
R206 4.7K_0402_5%
I2C_DAT, I2C_CLK
I2C_DAT <29>, I2C_CLK <29>
MEMID0 R207 10K_0402_5% X76@ +3VS
MEMID1 R208 10K_0402_5% X76@
MEMID2 R209 10K_0402_5% X76@

CRT

R	AK24	VGA_CRT_R	VGA_CRT_R <28>
G	AM24	VGA_CRT_G	VGA_CRT_G <28>
B	AL24	VGA_CRT_B	VGA_CRT_B <28>
HSYNC	AJ23	CRT_HSYNC	CRT_HSYNC <28>
VSYNC	AJ22	CRT_VSYNC	CRT_VSYNC <28>

Need Level Shift

R213 4.7K_0402_5%
R214 4.7K_0402_5%
Need Level Shift
DDC1DATA AH22 VGA_CRT_DAT → VGA_CRT_DAT <28>
DDC1CLK AH23 VGA_CRT_CLK → VGA_CRT_CLK <28>
GENERICA AK22
GENERICB AF23 R216 1K_0402_5%
GENERICA NC,GENERICB Grounded -->Internal SS LVDS Bus
RSET AL22 R219 499_0402_1%

TV

R2 AK15
G2 AM15
B2 AL15
H2SYNC AF15
V2SYNC AG15
Y AJ15 VGA_TV_Y → VGA_TV_Y <28>
C AJ13 VGA_TV_C → VGA_TV_C <28>
COMP AH15 VGA_TV_COMP → VGA_TV_COMP <28>
R2SET AK14 R223 715_0402_1%
ROMCS# AC7
PLLTEST AG14
TESTEN AG22 R228 1K_0402_5%

Straps: (Internal pull down)

Transmitter power saving enable	*GPIO[0]*	*0: 50% TX output swing* *1: Full TX output swing*
Transmitter de-emphasis enable	*GPIO[1]*	*0: TX de-emphasis disable* *1: TX de-emphasis enable*
Debug Access	*GPIO[4]*	*0: OFF Pad must be available* *1: ON*
PLL_IBIAS_RD	*GPIO[6,5]*	*Default : 01*
ROM ID Config	*GPIO[9, 13:11]*	000X: No ROM, AP_SIZE=00 128M share 001X: No ROMMemory AP_SIZE=01 256M share 010X: No ROMMemory AP_SIZE=10 64M share 011X: No ROMMemory AP_SIZE=11 Reserved

Vedio Memory Config. (VGA Internal PD)

MEMID[2:0]	Size	Size	Vender	Chips	VGA	Frequence
0 0 0	64MB	16M16	Hynix	2		
0 0 1	64MB	16M16	Samsung	2		
0 1 0	128MB	16M16	Hynix	4		**A-test**
0 1 1	128MB	16M16	Samsung	4		
1 0 0	256MB	32M16	Hynix	4		**A-test**
1 0 1	256MB	32M16	Samsung	4		
1 1 0		Resreved				
1 1 1		Resreved				

TBD

Security Classification	Compal Secret Data		
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Title: SCHEMATIC, M/B LA-3151P

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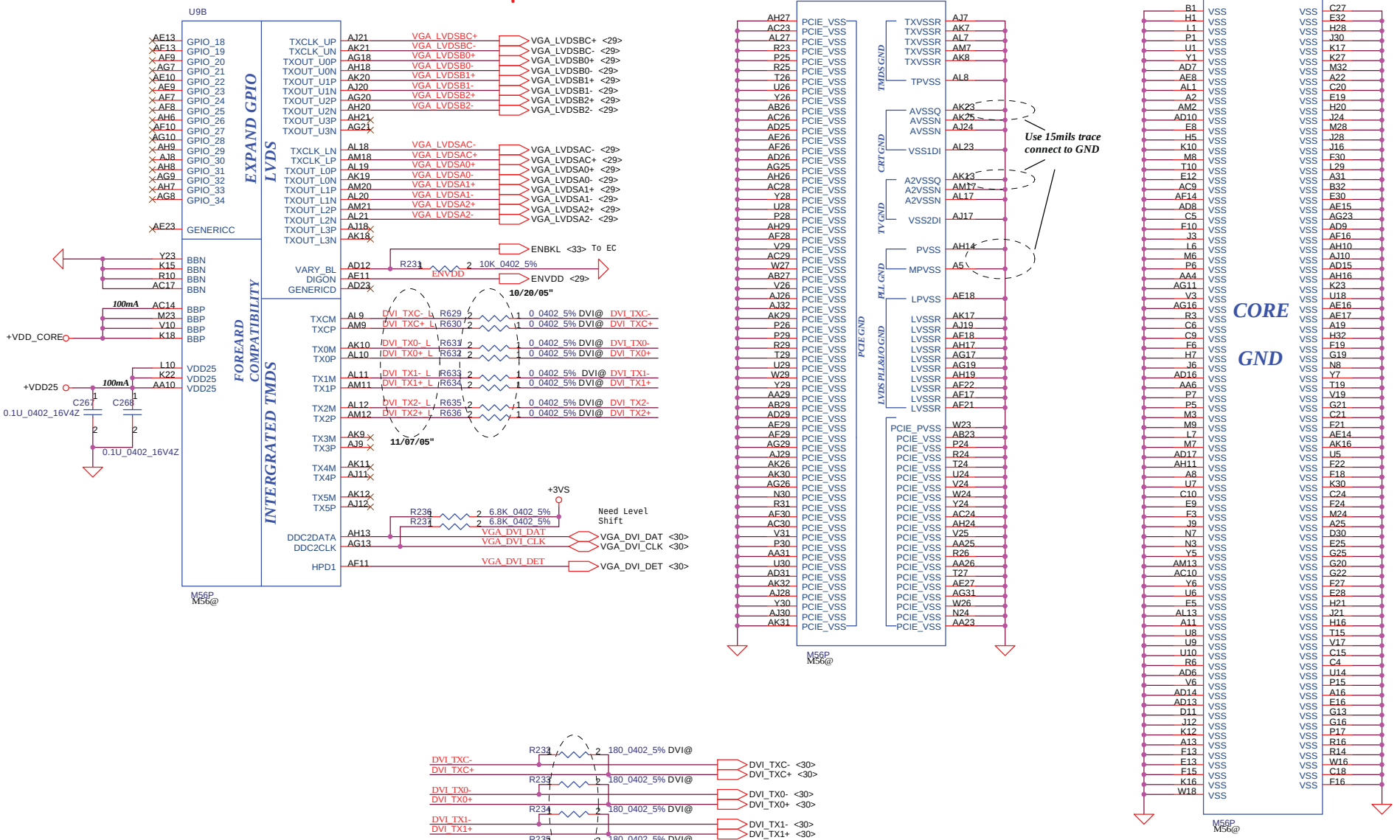

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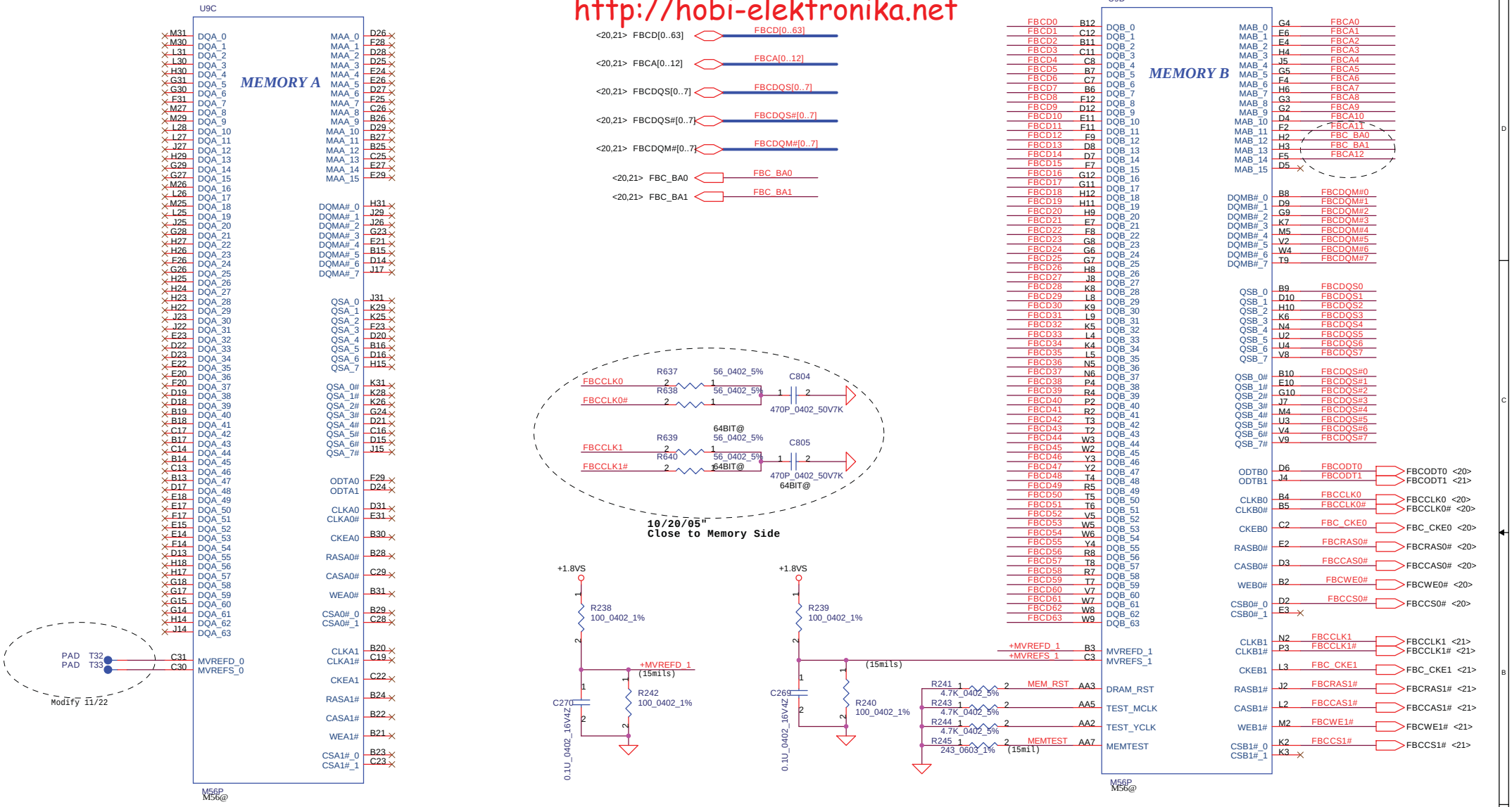

GDDR2

Security Classification	Compal Secret Data		
Issued Date	2005/09/10	Deciphered Date	2006/09/10

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Size	Document Number	Rev
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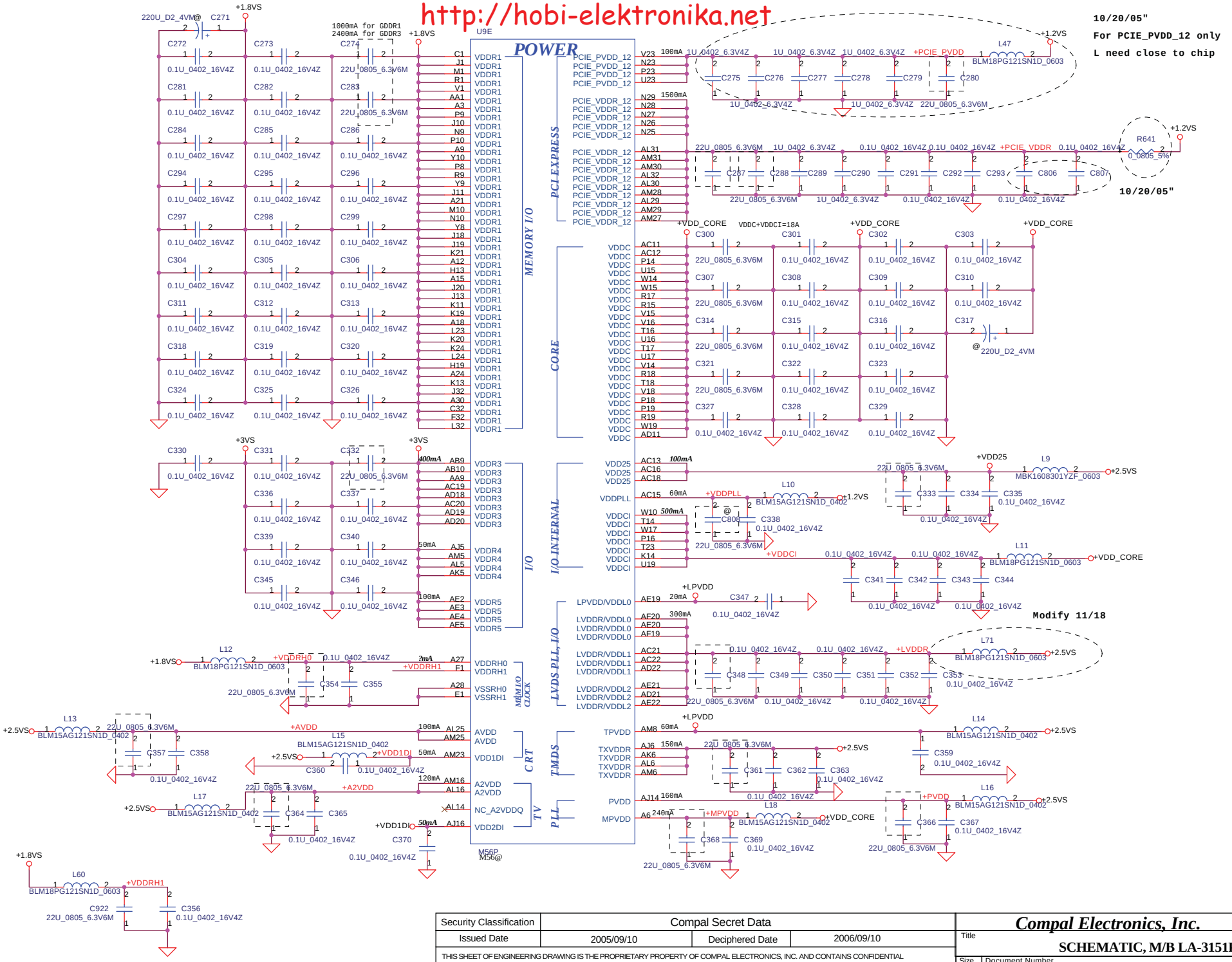

Security Classification	Compal Secret Data		
Issued Date	2005/09/10	Deciphered Date	2006/09/10

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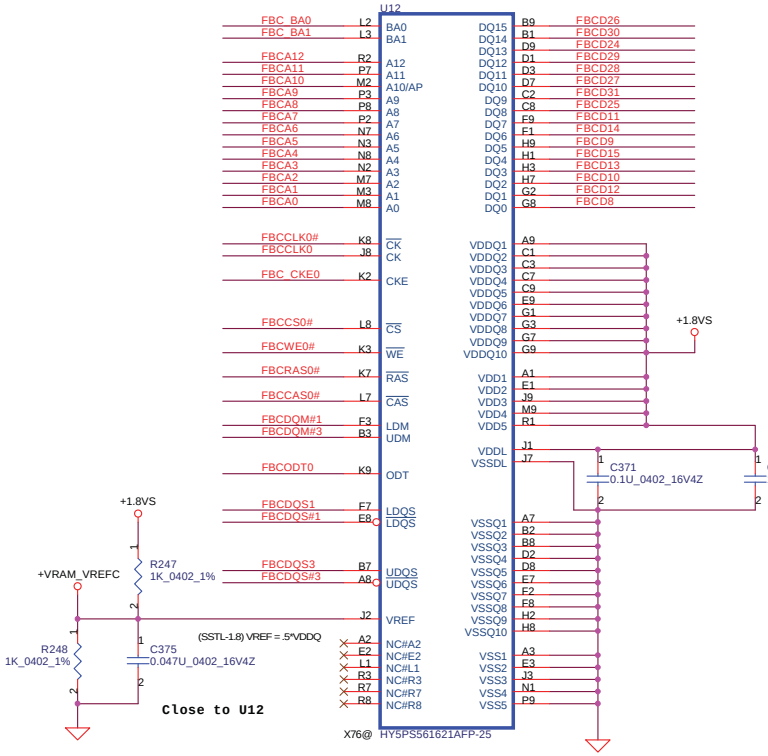
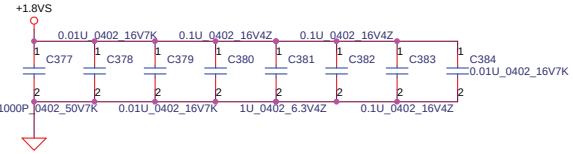
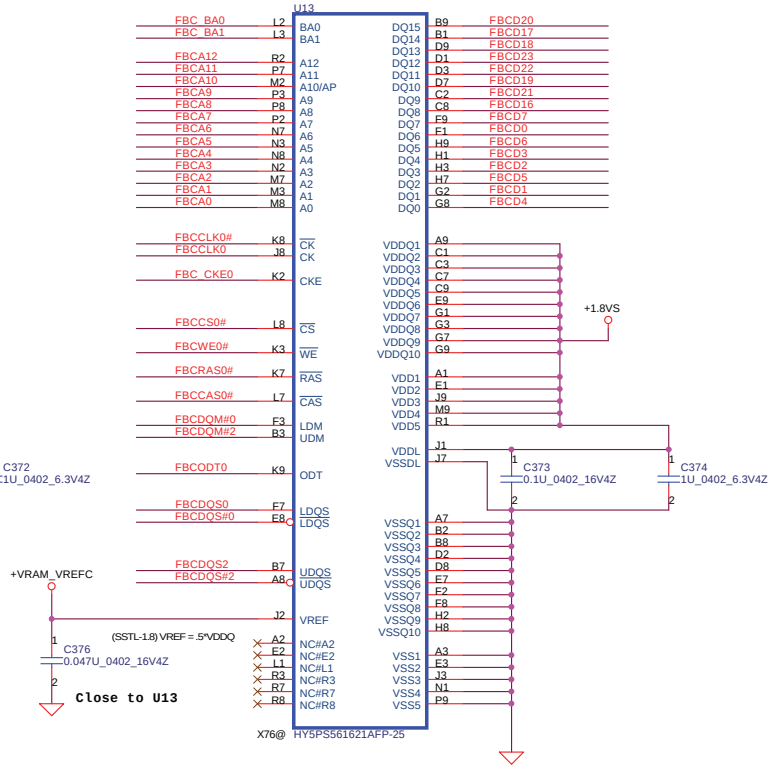
11/03/05' SWAP NET
11/04/05' SWAP NET
11/08/05' SWAP NET



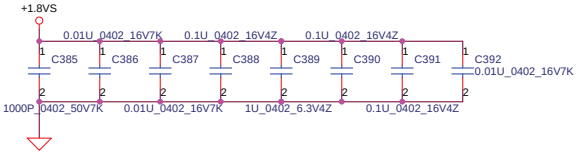
DDR2 BGA MEMORY

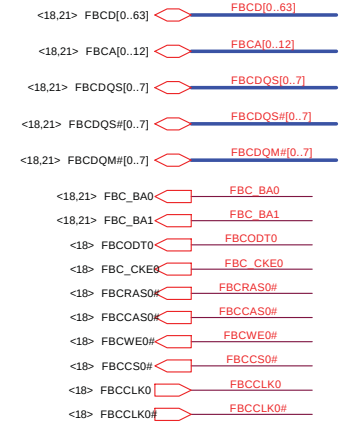


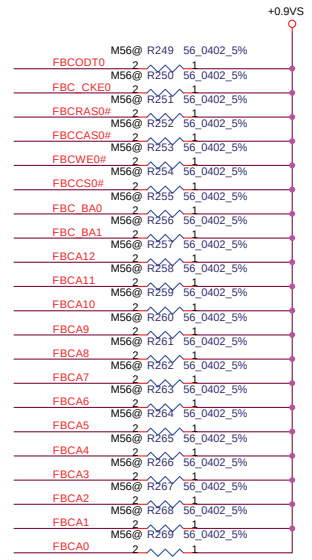
11/03/05' SWAP NET



DDR2 BGA MEMORY







M56 Only

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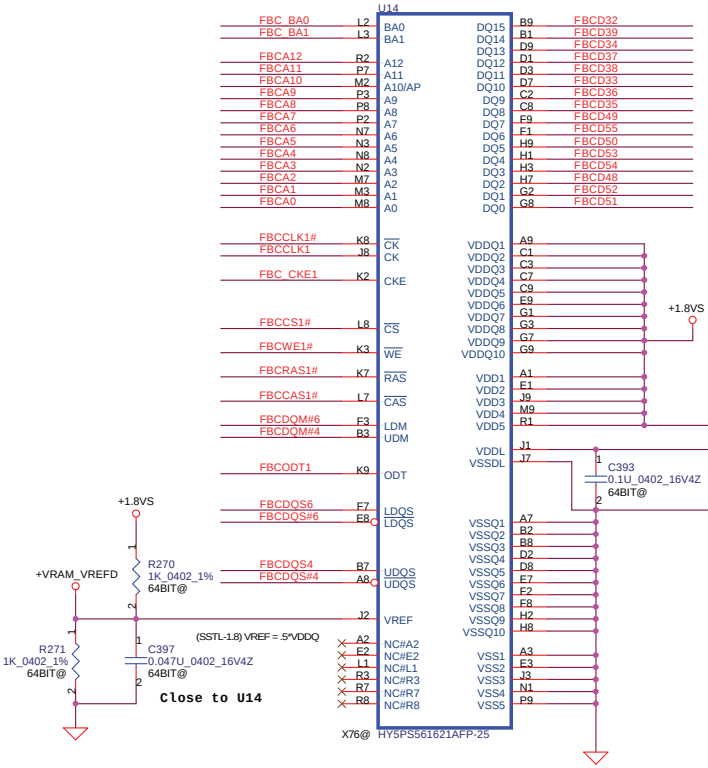
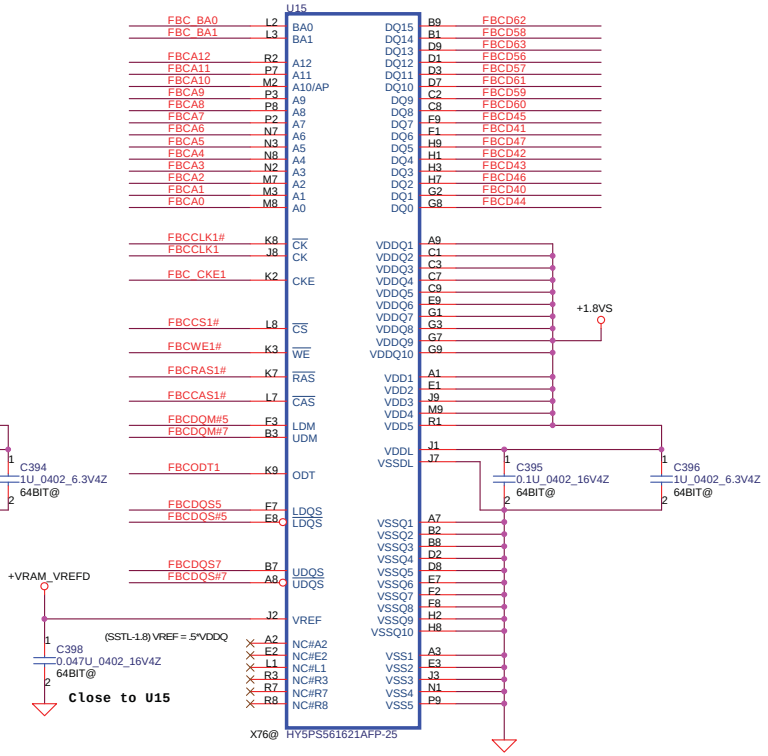
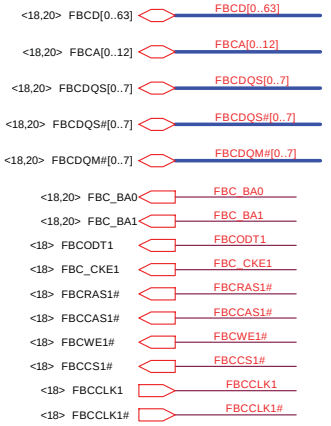
11/03/05' SWAP NET

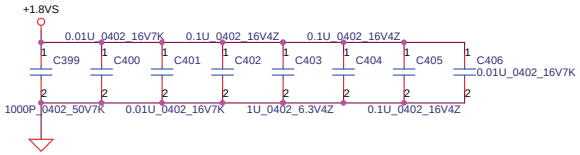


11/03/05' SWAP NET

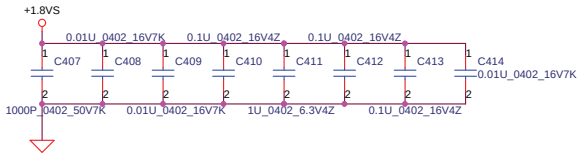


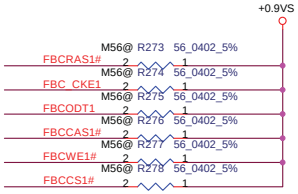


DDR2 BGA MEMORY



DDR2 BGA MEMORY





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Security Classification	Compal Secret Data		
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Title: SCHEMATIC, M/B LA-3151P

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

FOR SB600 VCC_SB= 1.2V
FOR SB460 VCC_SB= 1.8V

R294 CALRP: SB600=562R 1%, SB460=150R 1%
R295 CALRN: SB600=2.05K 1%, SB460=150R 1%
R296 CALRN: SB600=0R 1%, SB460=4.12K 1%

C608 AND C609 CLOSE TO U600.U29

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

FOR SB600, CONNECT TO CPU_PG/LDT_PG
FOR SB460, CONNECT TO SSMUXSEL/GPIO0

FOR SB460, THIS BALL IS LDT_RST# ONLY

SB460 ONLY

LPC PULL UPS

SB460 Part 1 of 4

218S4RASA11GS SB460_BGA549

EMI 11/2 Modify

RTC Battery

Please Closed RAM Door

Modify 11/07

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Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

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SB460 ONLY

+3VS
R309 2 1 10K_0402_5% LPC_SMI#
R310 2 1 10K_0402_5% EC_FLASH#_R
R644 2 1 10K_0402_5% SB_INT_FLASH_SEL#

+3VALW
R313 2 1 10K_0402_5% SYS_RESET#
R314 2 1 10K_0402_5% LPC_PME#
R315 2 1 @10K_0402_5% EC_KBRST#
R316 2 1 10K_0402_5% PBTN_OUT#
R318 2 1 10K_0402_5% EC_SWI#
R320 2 1 10K_0402_5% SB_PCIE_WAKE#
R322 2 1 4.7K_0402_5% PM_SLP_S5#
R323 2 1 4.7K_0402_5% PM_SLP_S3#
R324 2 1 4.7K_0402_5% S3_STATE_R
R325 2 1 10K_0402_5% EC_SCI#
R326 2 1 10K_0402_5% BLINK/GPM6#
R328 2 1 10K_0402_5% EC_SMI#
R329 2 1 10K_0402_5% USB_OC#0
R330 2 1 10K_0402_5% USB_OC#1
R331 2 1 10K_0402_5% USB_OC#3
R332 2 1 10K_0402_5% CP_PE#
R333 2 1 10K_0402_5% USB_OC#6

+3VS
R337 2 1 2.2K_0402_5% SB_CK_SCLK
R338 2 1 2.2K_0402_5% SB_CK_SDAT
R647 2 1 10K_0402_5% GPIO13
R831 2 1 10K_0402_5% IDE_HRESET#

<34> ICH_BITCLK_MDC R341 1 2 33_0402_1% AZ_BIT_CLK
<44> ICH_BITCLK_AUDIO R342 1 2 33_0402_1%
<34> ICH_SYNC_MDC R343 1 2 33_0402_1% AZ_SYNC
<44> ICH_SYNC_AUDIO R346 1 2 33_0402_1%
<34> ICH_RST_MDC# R347 1 2 33_0402_1% AZ_RST#
<44> ICH_RST_AUDIO# R348 1 2 33_0402_1%
<34> ICH_SDOUT_MDC R349 1 2 33_0402_1% AZ_SDATA_OUT
<44> ICH_SDOUT_AUDIO R350 1 2 33_0402_1%

R351 2 1 @10K_0402_5% ICH_AC_SDIN2
R352 2 1 @10K_0402_5% ICH_AC_SDIN1
R354 2 1 @10K_0402_5% ICH_AC_SDIN0

R355 2 1 10K_0402_5% AZ_RST#
R356 2 1 @10K_0402_5% AZ_SYNC
R357 2 1 @10K_0402_5% AZ_SDATA_OUT
R358 2 1 @10K_0402_5% AZ_BIT_CLK
R648 2 1 10K_0402_5% AC_RST#

ICH_BITCLK_MDC — C945 1 2 @10P_0402_50V8K
ICH_BITCLK_AUDIO — C946 1 2 @10P_0402_50V8K
Modify 11/27

<33> EC_SWI# EC_SWI# A3
<33> EC_SCI# EC_SCI# B2
<33> PM_SLP_S3# PM_SLP_S3# F7
<33> PM_SLP_S5# PM_SLP_S5# A5
<33> PBTN_OUT# PBTN_OUT# E3
<7,42> SB_PWRGD SB_PWRGD B5
<35> SUS_STAT# SUS_STAT# B3
R319 2 1 10K_0402_5%
R321 2 1 10K_0402_5%
<33> EC_GA20 EC_GA20 AF26
<33> EC_KBRST# EC_KBRST# AG26
Modify : 11/07
<33> S3_STATE R813 2 1 @0_0402_5% SYS_RESET# D9
<36,39> SB_PCIE_WAKE# SB_PCIE_WAKE# E7
<7> H_THERMTRIP# H_THERMTRIP# G7
<33> EC_RSMRST# EC_RSMRST# E2
<15> SB_OSCIN SB_OSC_INT B23
R334 2 1 10K_0402_5%
R335 2 1 10K_0402_5%
R336 2 1 10K_0402_5%
<35> EC_FLASH# R830 2 1 0_0402_5% +3VS
EC_FLASH# SB_INT_FLASH_SEL# D23
<44> SB_SPKR SPKR/GPIO2 B26
<9,10,15> SB_CK_SCLK SB_CK_SCLK C27
<9,10,15> SB_CK_SDAT SB_CK_SDAT B28
R339 2 1 10K_0402_5%
R340 2 1 10K_0402_5%
<7> CPU_PWRGD CPU_PWRGD A27
BALLS(C6 AND C5) ARE FOR SB600 ONLY (NC FOR SB460)
<33> EC_SMI# EC_SMI# C4
USB_OC#6 B4
AZ_RST# B6
<39> CP_PE# CP_PE# A6
EC_FLASH# R832 2 1 @0_0402_5% USB_OC#3 C8
<33> EC_LID_OUT# EC_LID_OUT# C7
USB_OC#1 B8
<39> USB_OC#0 USB_OC#0 A8
AZ_BIT_CLK N2
AZ_SDATA_OUT M2
AZ_SYNC L3
<26> AC_SDATA_OUT AC_SDATA_OUT L1
<44> ICH_AC_SDIN0 ICH_AC_SDIN0 L2
<34> ICH_AC_SDIN1 ICH_AC_SDIN1 J2
ICH_AC_SDIN2 J4
AC_RST# M3
SB460 ONLY
AC_RST# L5
R814 2 1 10K_0402_5%
<27> IDE_HRESET# IDE_HRESET# AC21
GPIO13 AD7
AE7
AA4
PAD T12
<7,33> EC_THERM# EC_THERM# T4
<7,13> LDT_STOP# R353 2 1 0_0402_5% D4
AB19
TEST POINT TP602 FOR SB460_FANOUT0

U16D
SB460 Part 4 of 4
PCI_PME#/GEVENT4# A3
RI#/EXTEVNT0# B2
SLP_S3# F7
SLP_S5# A5
PWR_BTN# E3
PWR_GOOD B5
SUS_STAT# B3
NC F9
TEST1 E9
TEST0 G9
GA20IN AF26
KBRST# AG26
LPC_PME#/GEVENT3# D7
LPC_SMI#/EXTEVNT1# C25
S3_STATE/GEVENT5# D9
SYS_RESET#/GPM7# F4
WAKE#/GEVENT8# E7
BLINK/GPM6# C2
SMBALERT#/THRMTRIP#/GEVENT2# G7
ACPI / WAKE UP EVENTS
RSMRST# E2
14M_OSC B23
OSC / RST
NC C28
ROM_CS#/GPIO1 A26
GHI#/GPIO6 B29
VGATE/GPIO7 A23
GPIO4 B27
GPIO5 D23
SPKR/GPIO2 B26
SCL0/GPOC0# C27
SDA0/GPOC1# B28
NC C3
NC F3
DDC1_SCL/GPIO9 D26
DDC1_SDA/GPIO8 C26
LDT_PG/SSMUXSEL/GPIO0 A27
NC A4
GPIO
NC C6
NC C5
USB_OC7#/GEVENT7# C4
USB_OC6#/GEVENT6# B4
USB_OC5#/AZ_RST#/GPM5# B6
USB_OC4#/GPM4# A6
USB_OC3#/GPM3# C8
USB_OC2#/FANOUT1/LLB#/GPM2# C7
USB_OC1#/GPM1# B8
USB_OC0#/GPM0# A8
USB OC
AZ_BITCLK N2
AZ_SDOUT M2
NC K2
AZ_SYNC L3
NC K3
AZALIA
AC_BITCLK/GPIO38 L1
AC_SDOUT/GPIO39 L2
ACZ_SDIN0/GPIO42 L4
ACZ_SDIN1/GPIO43 J2
ACZ_SDIN2/GPIO44 J4
AC_SYNC/GPIO40 M3
AC_RST#/GPIO45 L5
AC97
FANOUT0/GPIO3 E23
GPIO31 AC21
GPIO13 AD7
DPSLP_OD#/GPIO37 AE7
GPIO14 AA4
TALERT#/GPIO10 T4
SLP#/LDT_STP# D4
NC AB19
218S4RASA11GS SB460_BGA549

USB INTERFACE
USBCLK A17 CLK_USB_48M
RCOMP A14 R312 2 1 11.3K_0402_1%
01/03/05" modify
ATEST1 A11
ATEST0 A10
NC H12
NC G12
NC E12
NC D12
SB600 ONLY
(NC for SB460)
HSDP7+ E14
HSDM7- D14
HSDP6+ G14 USB20_P6 USB20_P6 <43>
HSDM6- H14 USB20_N6 USB20_N6 <43>
HSDP5+ D16 USB20_P5 USB20_P5 <34>
HSDM5- E16 USB20_N5 USB20_N5 <34>
HSDP4+ D18 USB20_P4 USB20_P4 <36>
HSDM4- E18 USB20_N4 USB20_N4 <36>
HSDP3+ G16 USB20_P3 USB20_P3 <43>
HSDM3- H16 USB20_N3 USB20_N3 <43>
HSDP2+ G18 USB20_P2 USB20_P2 <39>
HSDM2- H18 USB20_N2 USB20_N2 <39>
HSDP1+ D19 USB20_P1 USB20_P1 <39>
HSDM1- E19 USB20_N1 USB20_N1 <39>
HSDP0+ G19 USB20_P0 USB20_P0 <39>
HSDM0- H19 USB20_N0 USB20_N0 <39>

USB PWR
AVDDTX_0 B9
AVDDTX_1 B11
AVDDTX_2 B13
AVDDTX_3 B16
AVDDTX_4 B18
AVDDRX_0 A9
AVDDRX_1 B10
AVDDRX_2 B12
AVDDRX_3 B14
AVDDRX_4 B17
AVDDC A12
AVSSC A13
AVSS_USB_1 A16
AVSS_USB_2 C9
AVSS_USB_3 C10
AVSS_USB_4 C11
AVSS_USB_5 C12
AVSS_USB_6 C13
AVSS_USB_7 C14
AVSS_USB_8 C16
AVSS_USB_9 C17
AVSS_USB_10 C18
AVSS_USB_11 C19
AVSS_USB_12 C20
AVSS_USB_13 D11
AVSS_USB_14 D21
AVSS_USB_15 E11
AVSS_USB_16 F21
AVSS_USB_17 F11
AVSS_USB_18 F12
AVSS_USB_19 E14
AVSS_USB_20 F16
AVSS_USB_21 F18
AVSS_USB_22 F19
AVSS_USB_23 F21
AVSS_USB_24 G11
AVSS_USB_25 G21
AVSS_USB_26 H11
AVSS_USB_27 H21
AVSS_USB_28 J11
AVSS_USB_29 J12
AVSS_USB_30 J14
AVSS_USB_31 J16
AVSS_USB_32 J18
AVSS_USB_33 J19

AVDD_USB — L21 — +3VALW
C435 C436 C437 C438 C439 C440 C441 C442 KC FBM-L11-201209-221LMAT_0805
10U_0805_10V4Z 10U_0805_10V4Z 1U_0402_6.3V4Z 1U_0402_6.3V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z
+3.3V_AVDDC — L22 — +3VALW
C443 C444 C445 KC FBM-L11-201209-221LMAT_0805
0.1U_0402_16V4Z 2.2U_0603_6.3V6K 1U_0402_6.3V4Z
PLACE C443,C444 AND C445 CLOSE TO U16

Security Classification	Compal Secret Data		
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Title: SCHEMATIC, M/B LA-3151P
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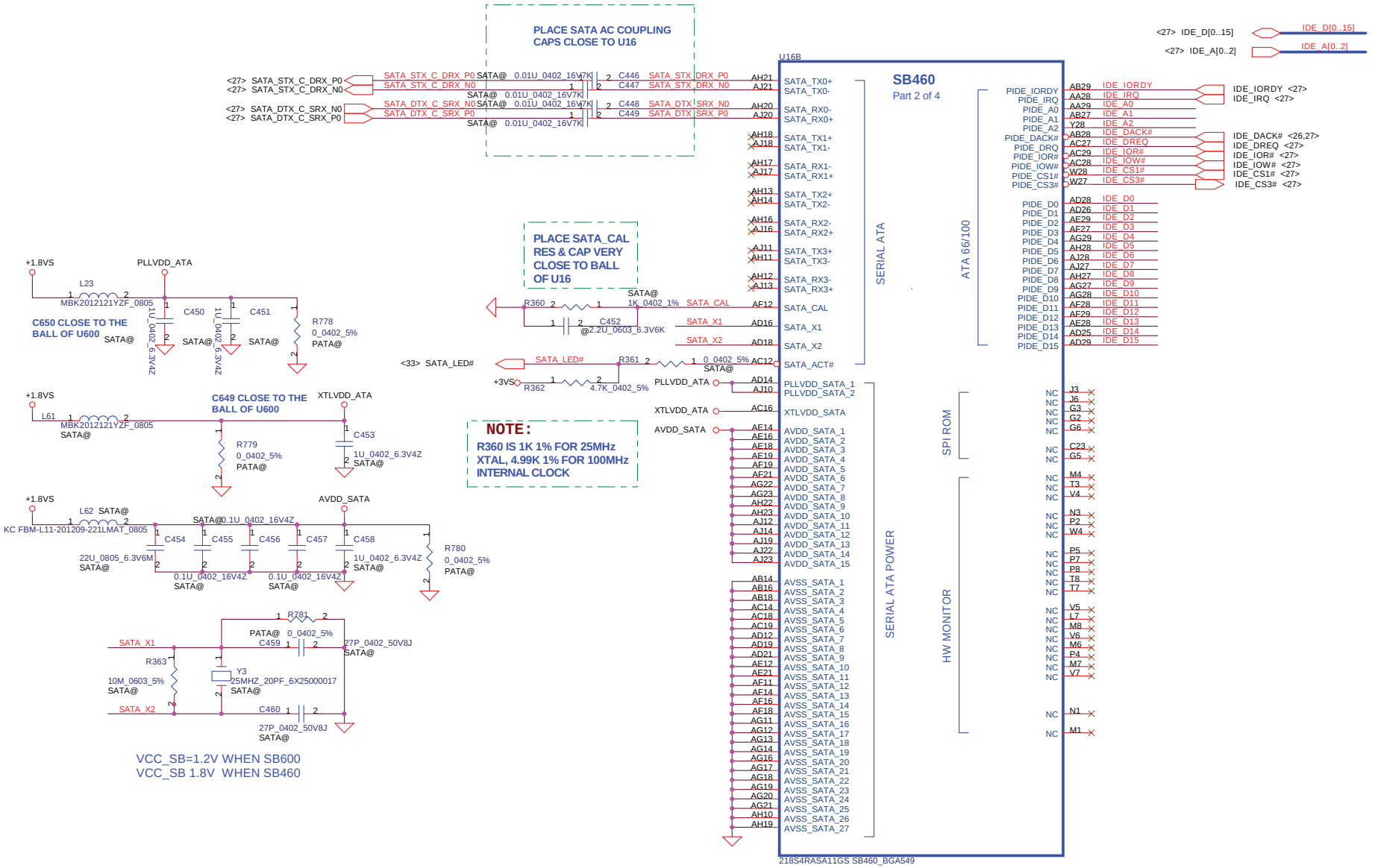

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Size	Document Number	Rev
Custom	401412	B

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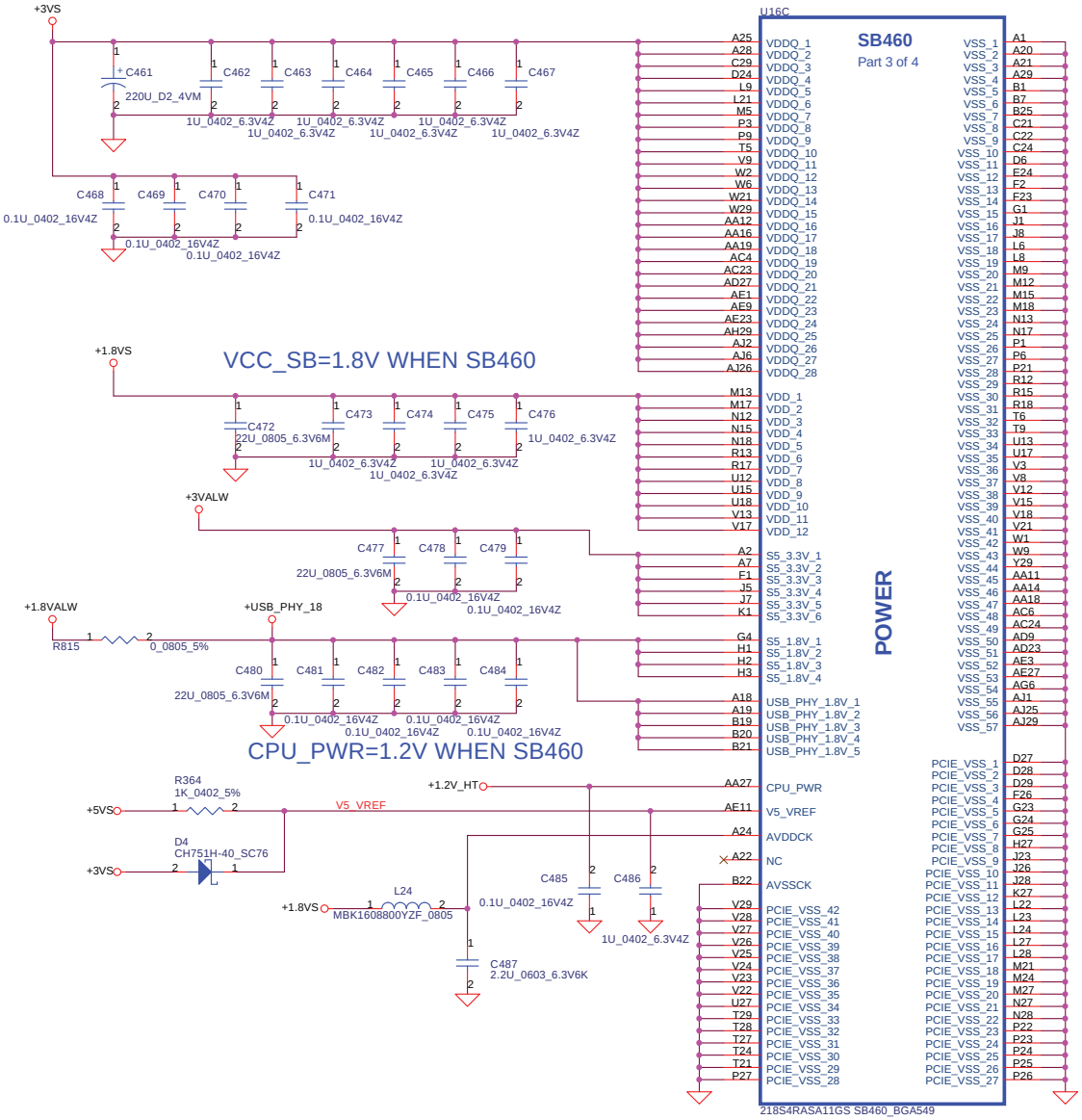

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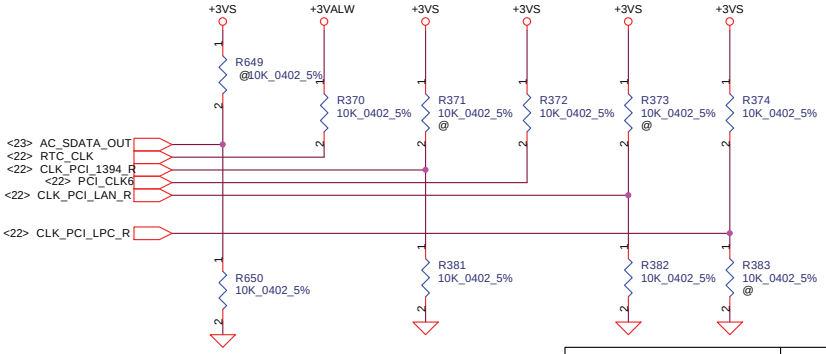
REQUIRED STRAPS

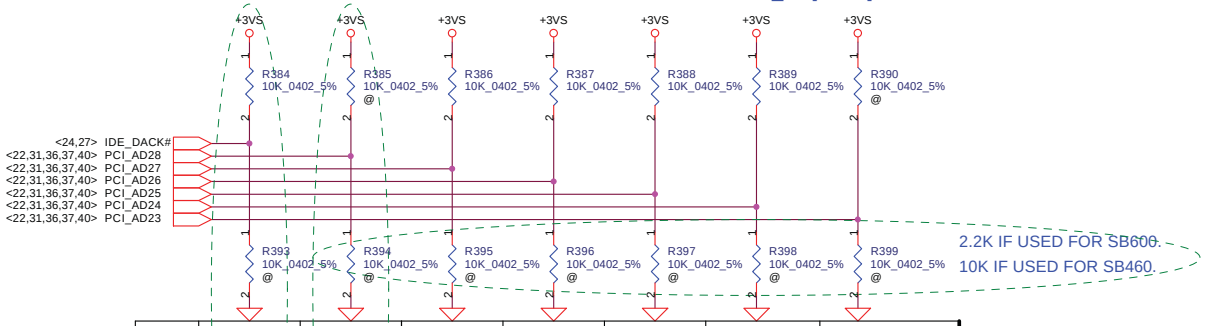
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



	AC_SDATA_OUT	RTC_CLK	PCI_CLK4 CLK_PCI_1394	PCI_CLK6	SB600 PCI_CLK0 CLK_PCI_LAN	SB600 PCI_CLK1 CLK_PCI_LPC	SB460 PCI_CLK0 CLK_PCI_LAN	SB460 PCI_CLK1 CLK_PCI_LPC
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM		ROM TYPE: H, H = PCI ROM; H, L = LPC I ROM; L, H = LPC II ROM DEFAULT; L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4			NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

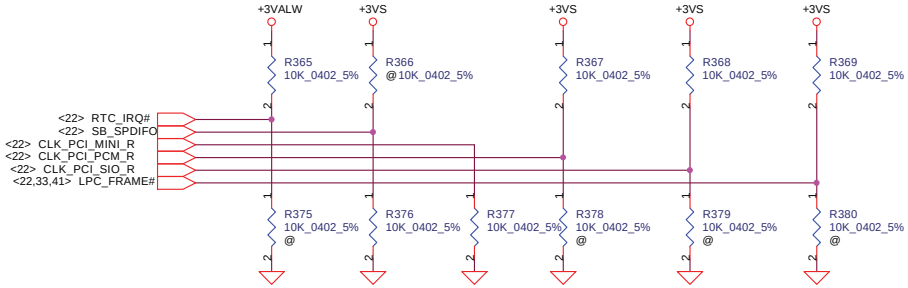
SB460 ONLY — SB600 ONLY

SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

NOTE: R365 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB460 TO KEEP THE INPUT FROM FLOATING.

SB460 ONLY



	ACPWRON RTC_IRQ#	SPDIF_OUT SB_SPDIFO	PCI_CLK2 CLK_PCI_MINI	PCI_CLK3 CLK_PCI_PCM	PCI_CLK5 CLK_PCI_SIO	LFRAME# LPC_FRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

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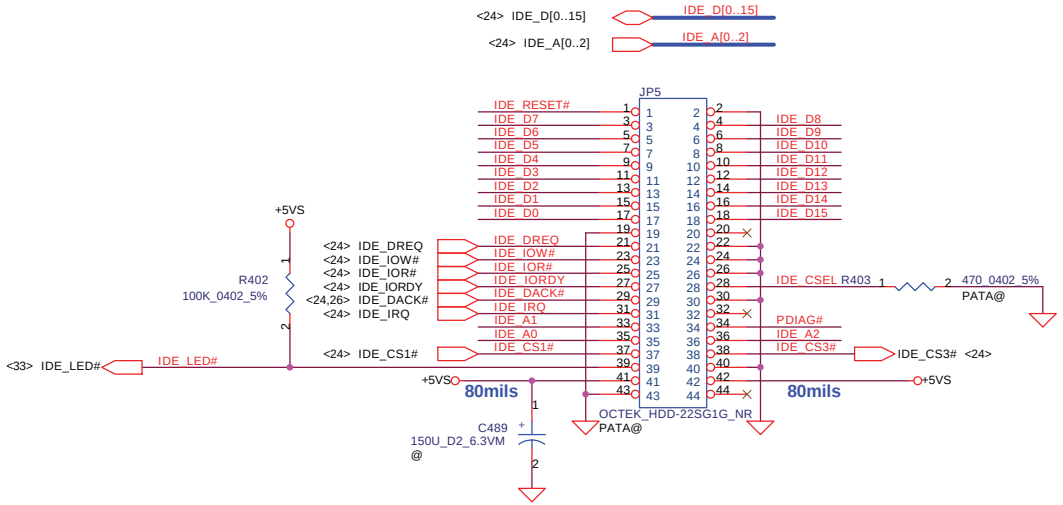
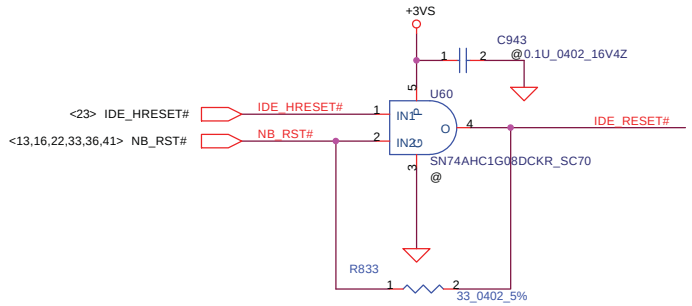
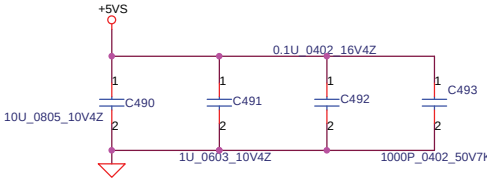
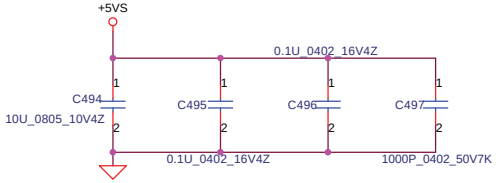
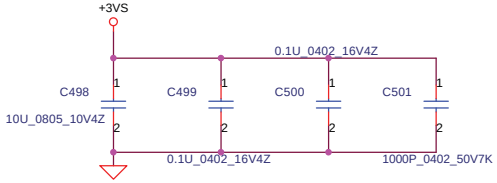
HDD CONN



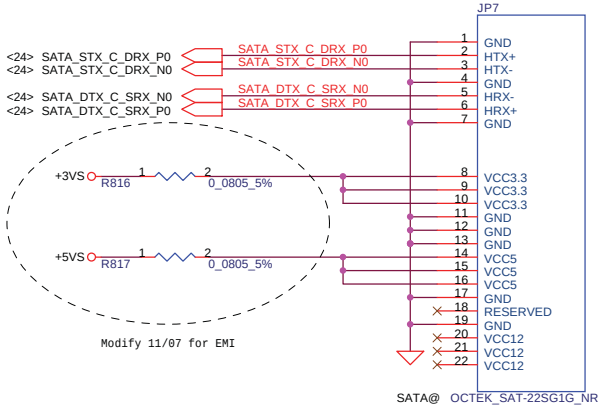






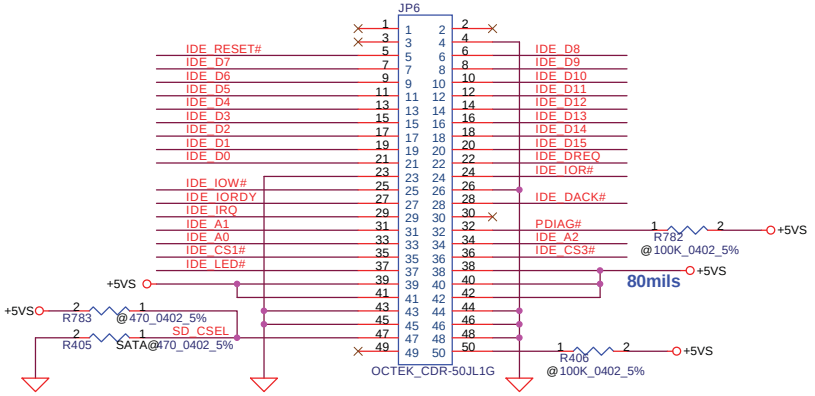


SATA HDD Conn.



(NEW)

CDROM CONN



IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

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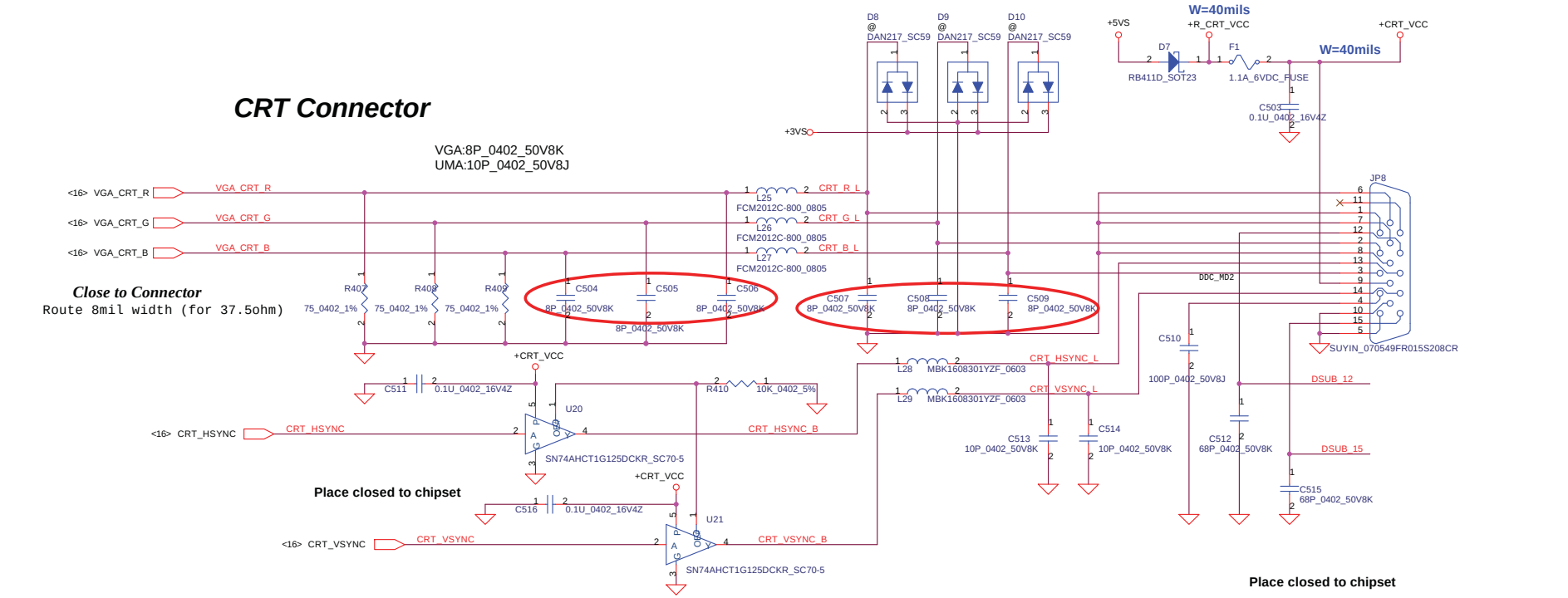

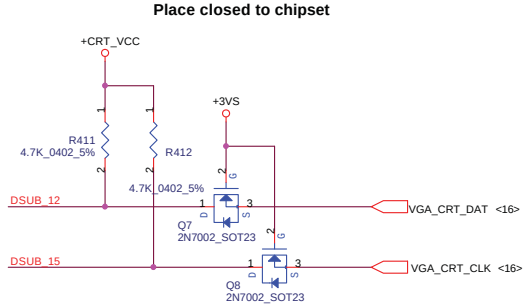

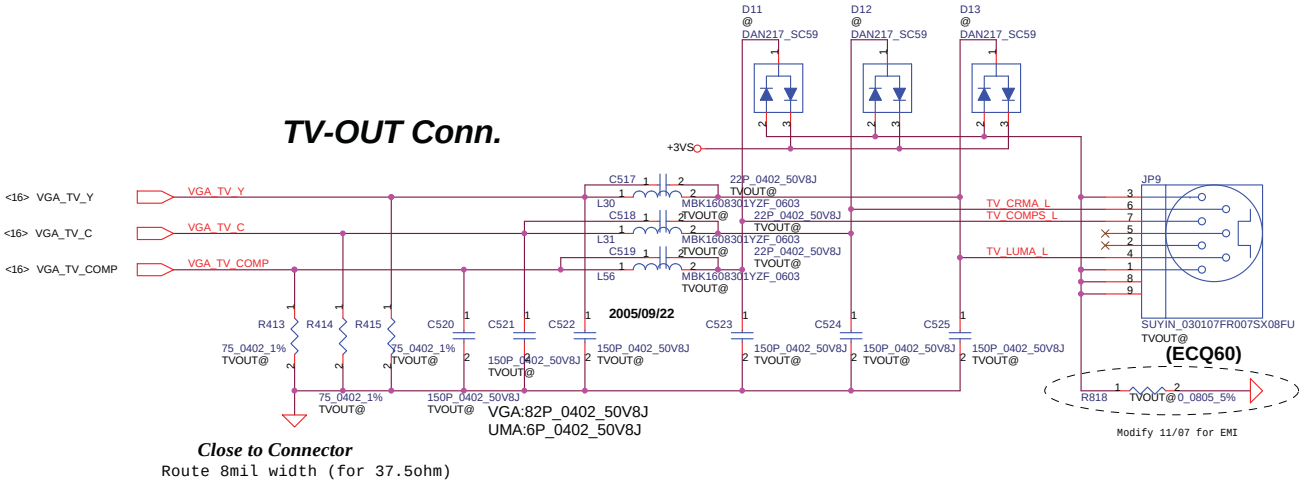

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Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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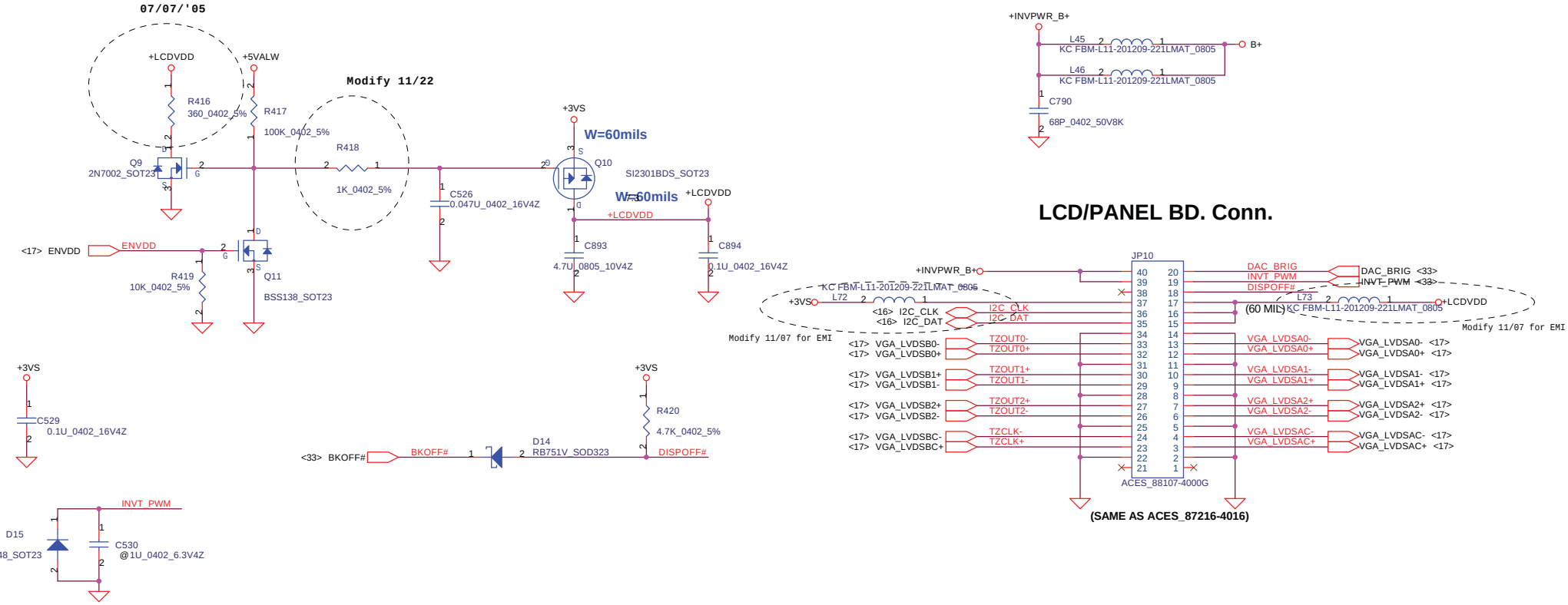
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

(SAME AS ACES_87216-4016)

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

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H5 H_C177D144 @
H30 H_C177D144 @
H20 H_C163D163N @

H1 H_S394D138 @
H2 H_S394D138 @
H4 H_S394D138 @
H21 H_S394D138 @
H22 H_S394D138 @

H23 H_S394D138 @
H14 H_S394D138 @
H15 H_S394D138 @
H28 H_S394D138 @
H7 H_C236D165 @

H8 H_C236D165 @
H9 H_C236D165 @
H10 H_C236D165 @
H3 H_C236D161 @
H6 H_C236D161 @

H29 H_C236D161 @
H31 H_S315D118 @
H11 H_O134X118D55X39 @
H12 H_O134X118D55X39 @
H17 H_O134X118D55X39 @

H18 H_O134X118D55X39 @
H16 H_C276D118 @
H19 H_C276D118 @
H13 H_S354D138 @
H24 H_S354D138 @

H25 H_S354D138 @
H32 H_S315D138 @
H33 H_C315D236 @
H34 H_O217X157D217X157N @

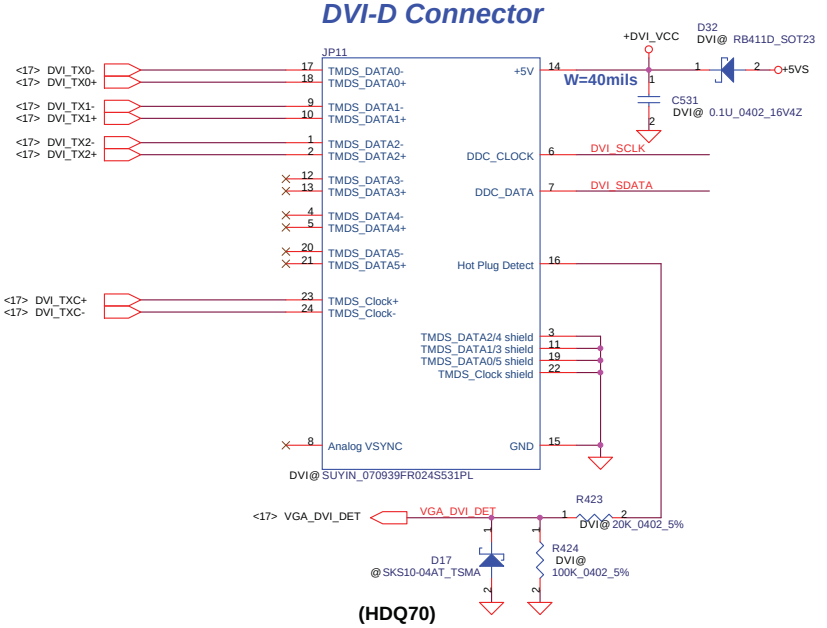
FD2 @ FD1 @ FD3 @ FD5 @ FD4 @ FD6 @

CF20 @ CF14 @ CF18 @ CF21 @ CF7 @ CF10 @ CF12 @ CF4 @ CF6 @ CF15 @

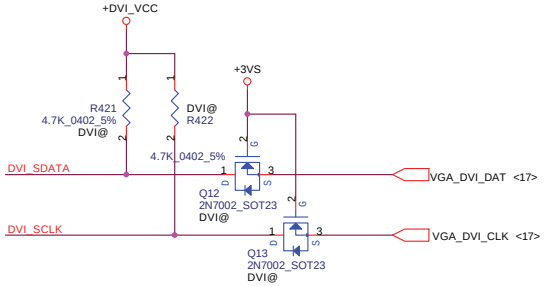
CF17 @ CF16 @ CF19 @ CF13 @ CF9 @ CF1 @ CF2 @ CF3 @ CF5 @ CF11 @

CF8 @ CF22 @ CF23 @ CF24 @

DVI-D Connector



(HDQ70)



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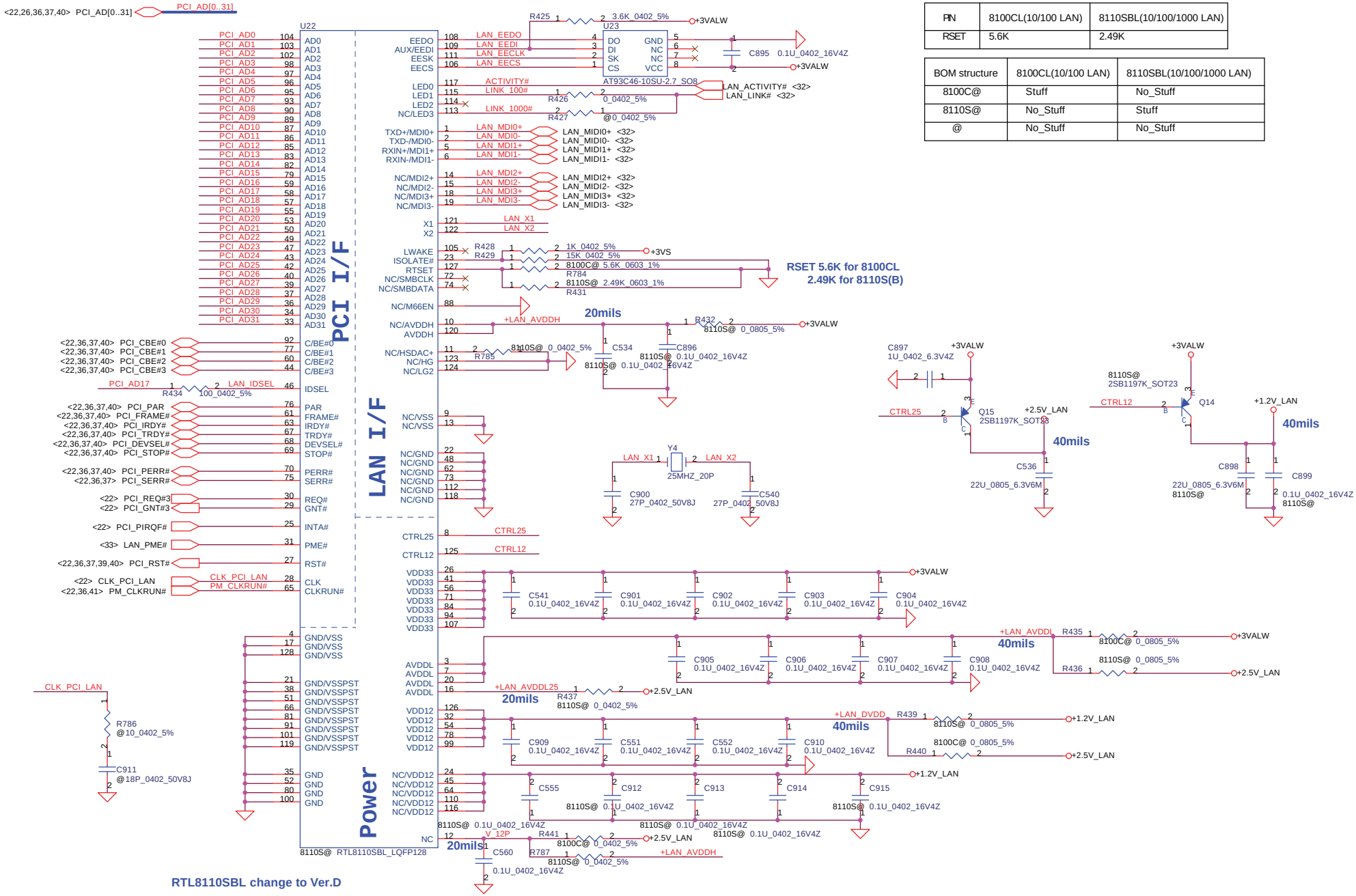

PIN	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
RSET	5.6K	2.49K

BOM structure	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
8100C@	Stuff	No_Stuff
8110S@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

Security Classification	Compal Secret Data		
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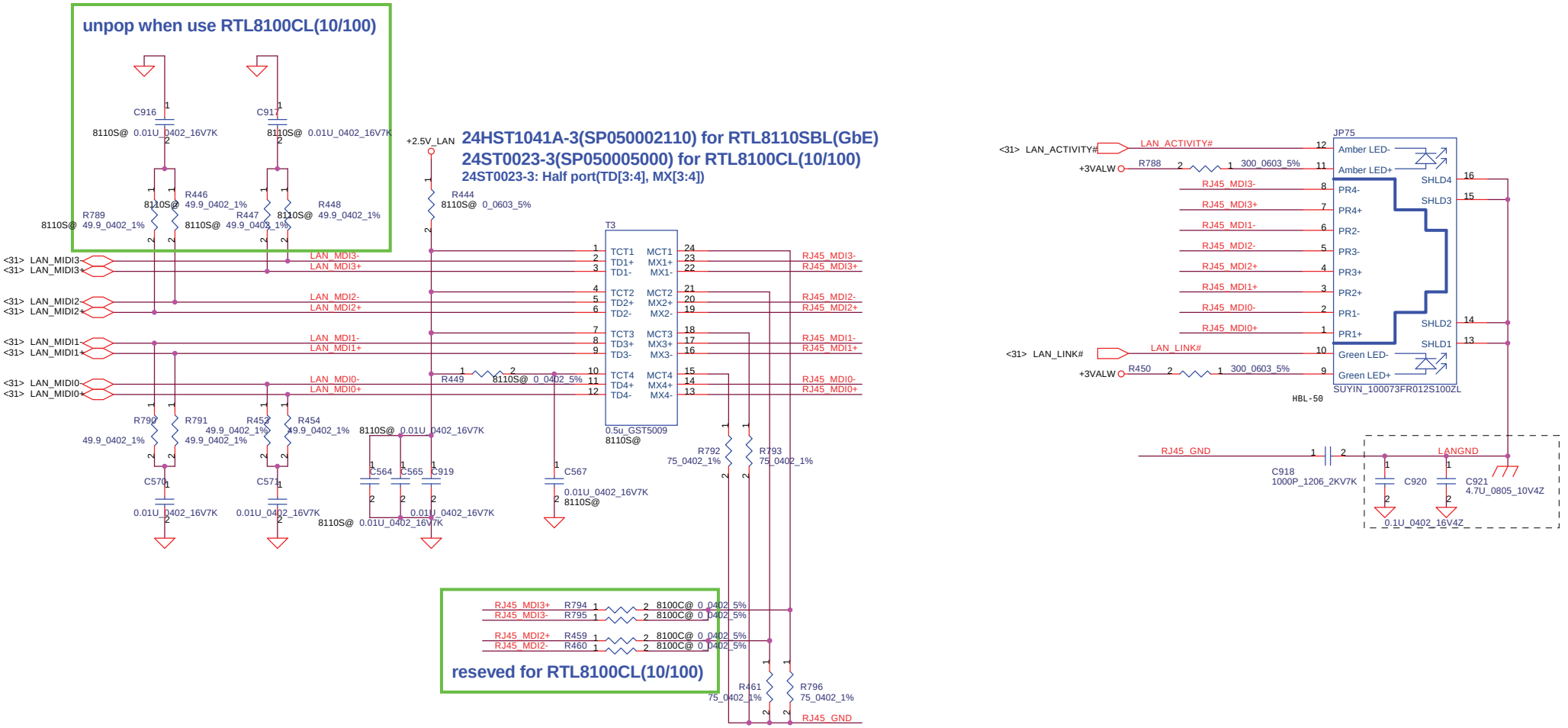
LAN RTL8110SBL/RTL8100CL



Security Classification	Compal Secret Data		
Issued Date	2005/07/29	Deciphered Date	2006/07/29

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ENE-KB910-B4

KB910 C1 VERSION

For EC Tools

Board ID	Ra	Rb	SATA Status	Rc	Rd
VGA	V	X	W/S SATA	V	X
UMA	X	V	W/O SATA	X	V

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

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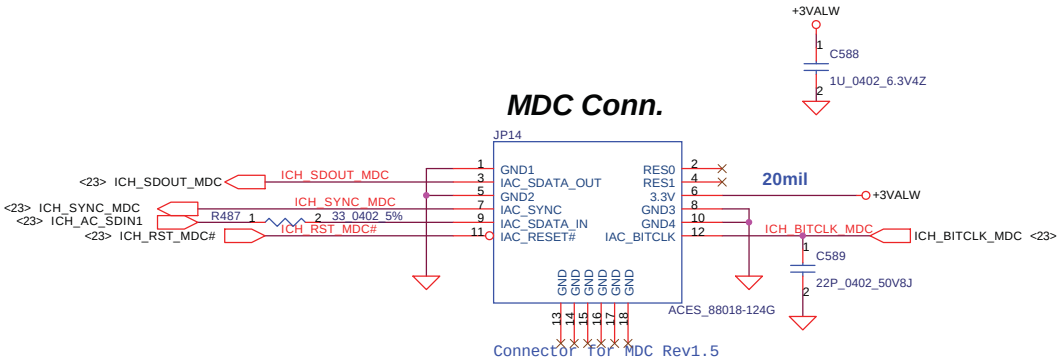
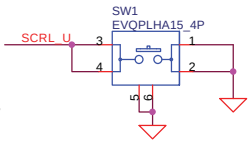
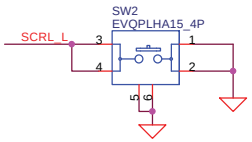
MDC Conn.



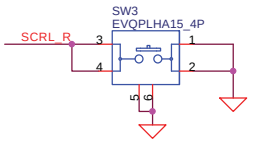
Scroll Up

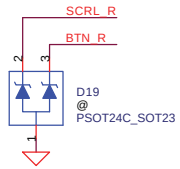


Scroll Left

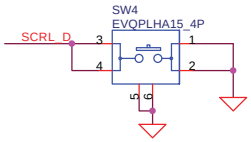


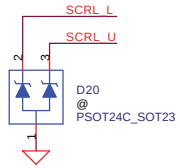
Scroll Right





Scroll Down





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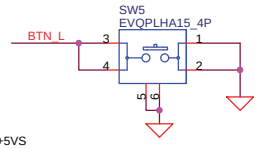

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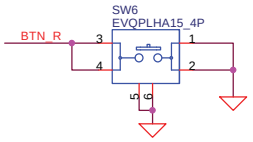
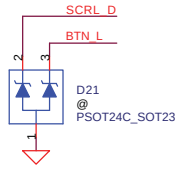
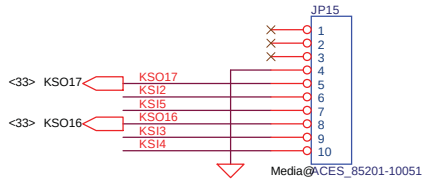




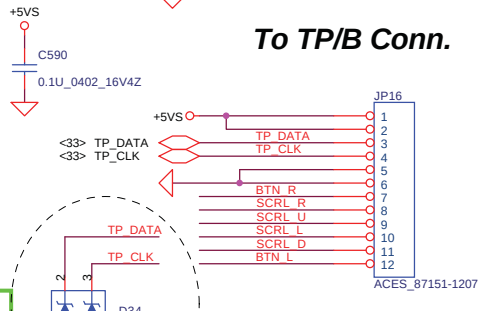
2005/09/04

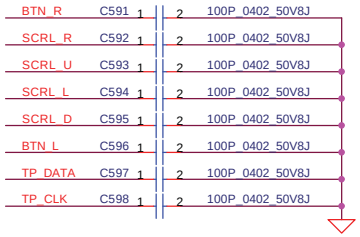


KSI[0..7] KSI[0..7] <33>

KSO[0..15] KSO[0..15] <33>

To TP/B Conn.





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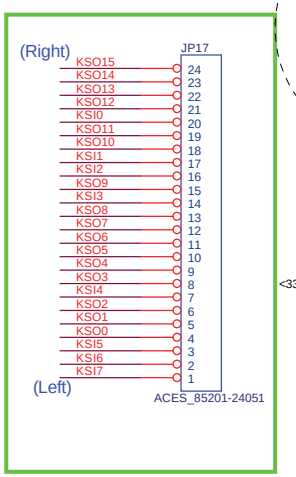
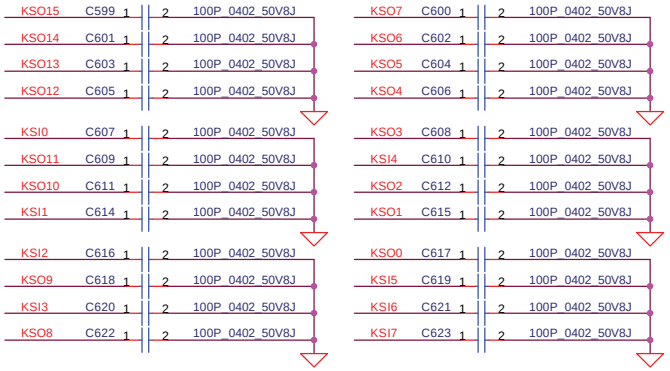
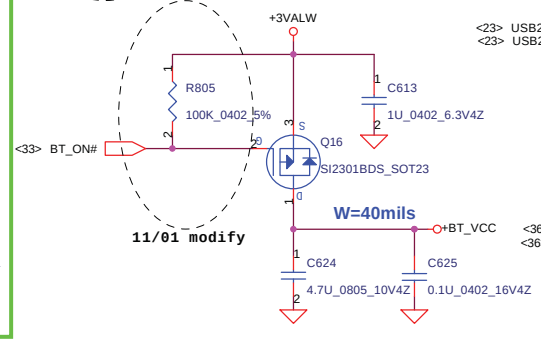
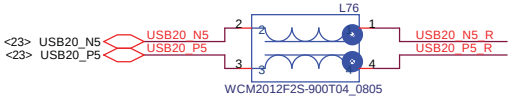
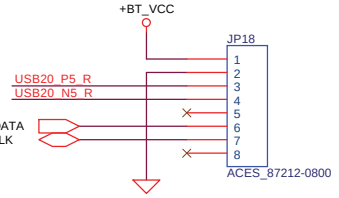




Bluetooth Conn.







Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

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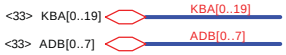

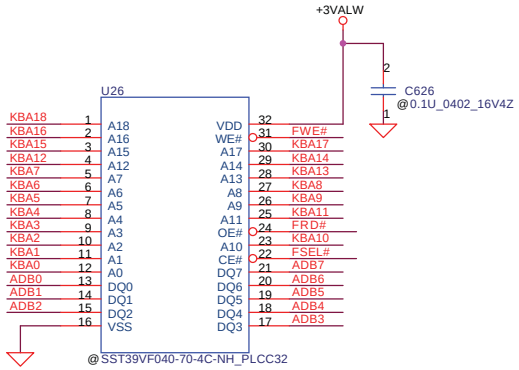

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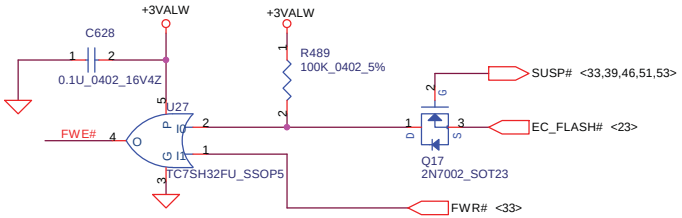
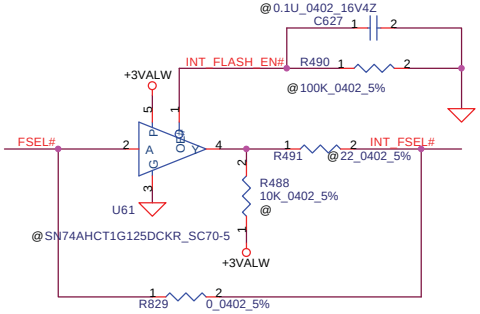
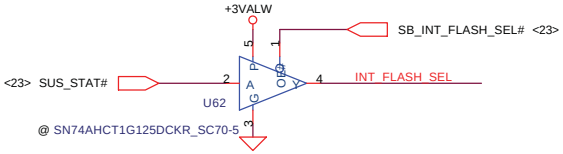
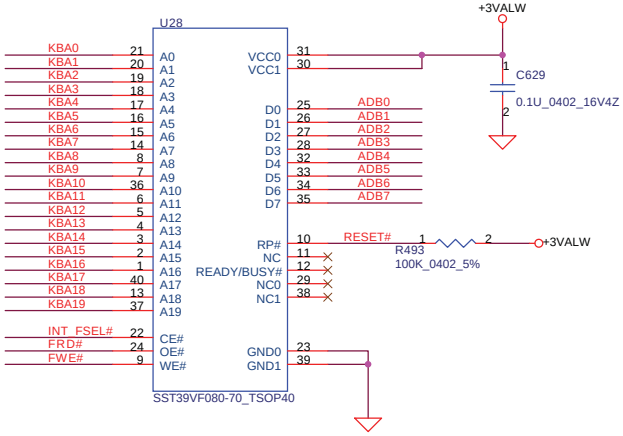




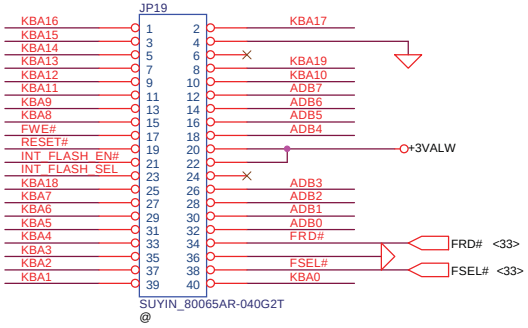
FOR DEBUG ONLY

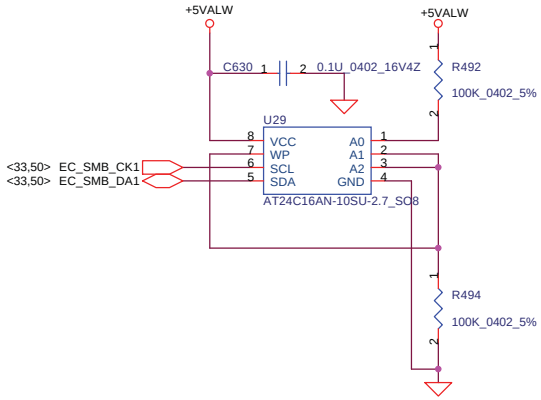


1MB Flash ROM



1MB Flash ROM





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Size	Document Number	Rev
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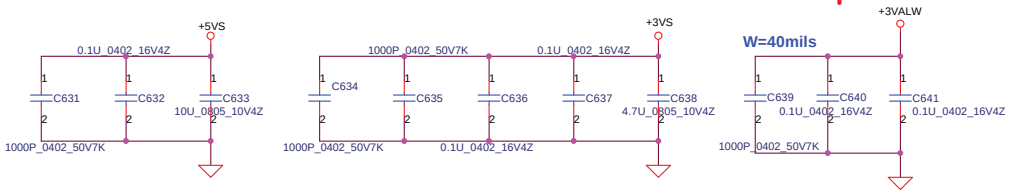

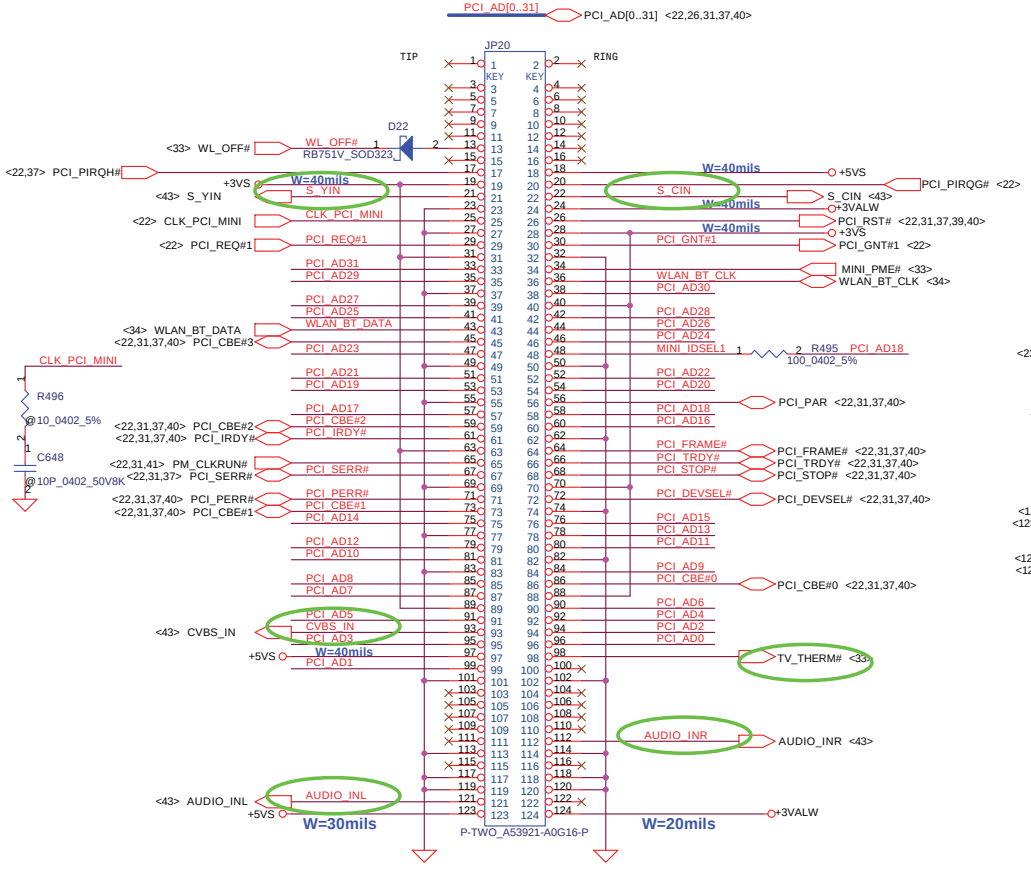

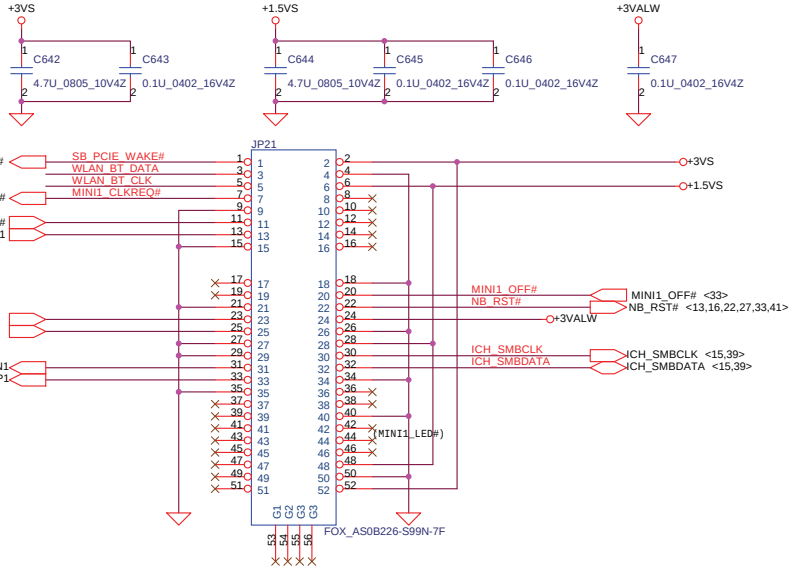

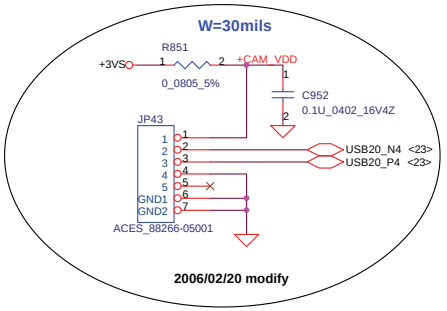

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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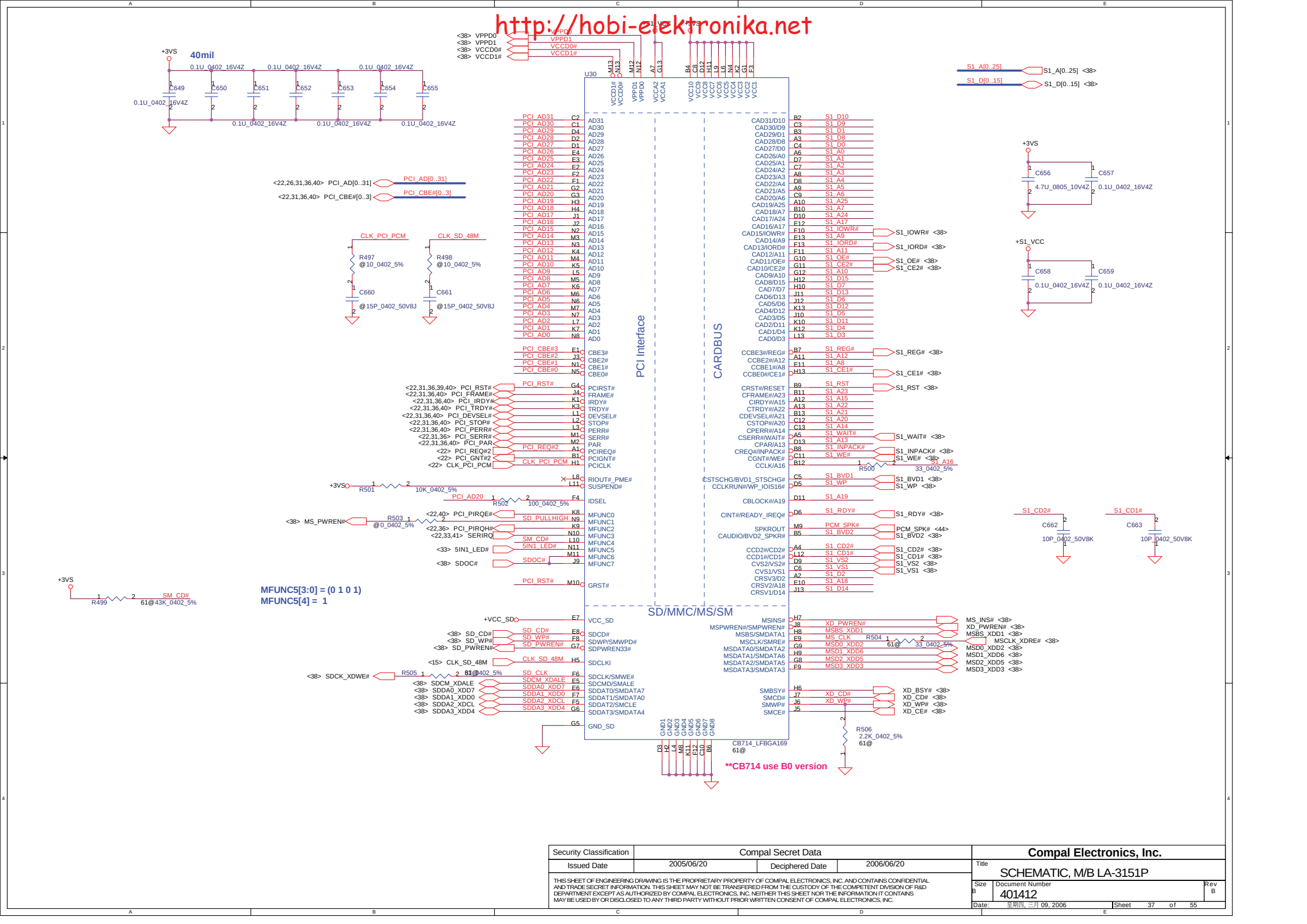

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Compal Electronics, Inc.

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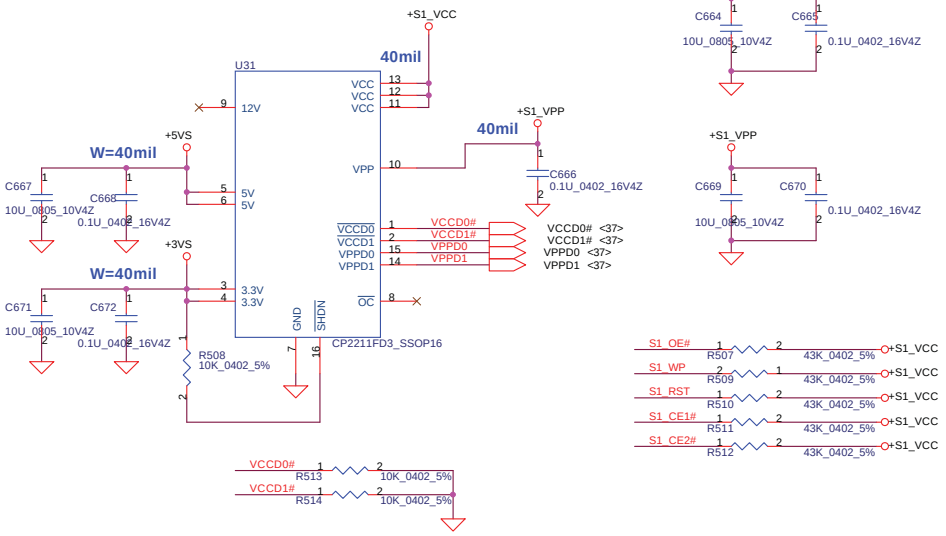
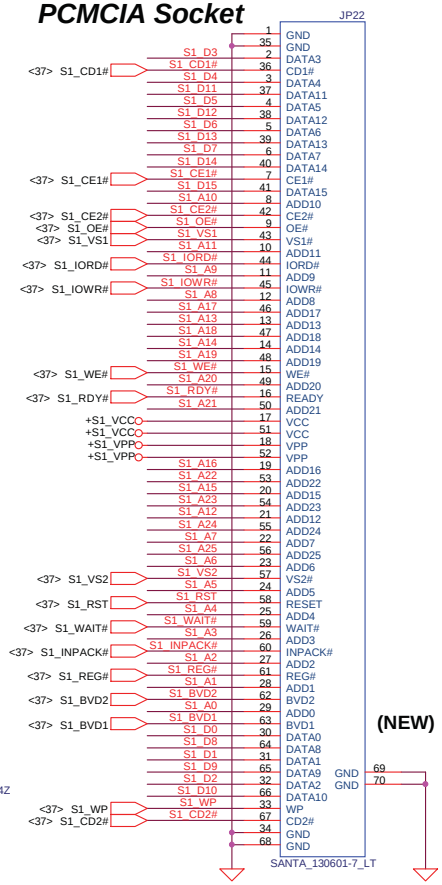
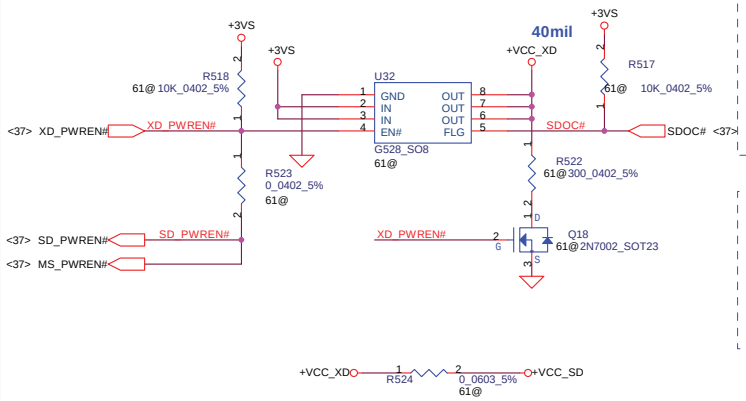
PCMCIA Power Control



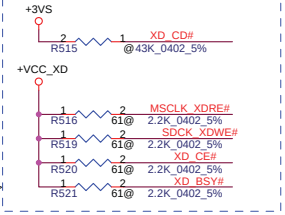
PCMCIA Socket



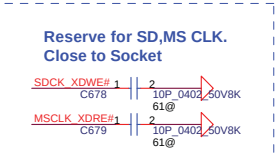
SD/MS Power Control
XD Power Control



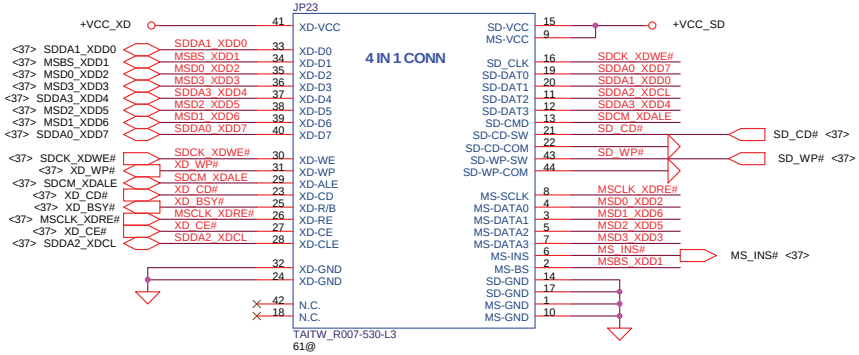
xD PU and PD. Close to Socket



Reserve for SD,MS CLK. Close to Socket



4 IN 1 Socket
(HDQ70)



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Issued Date	2005/06/20	Deciphered Date	2006/06/20

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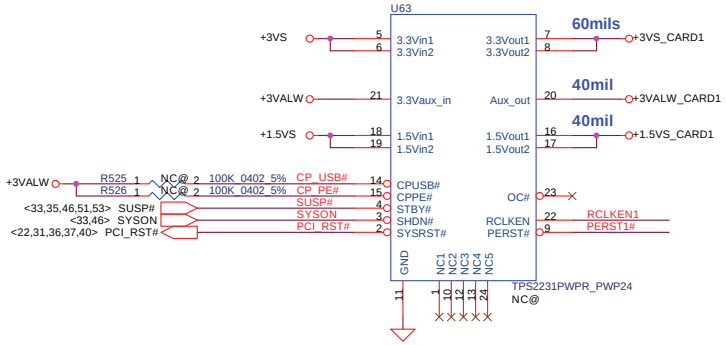
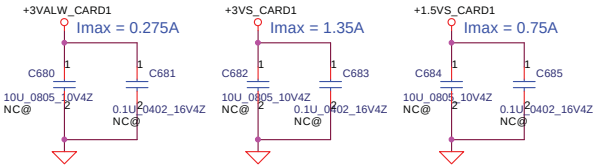
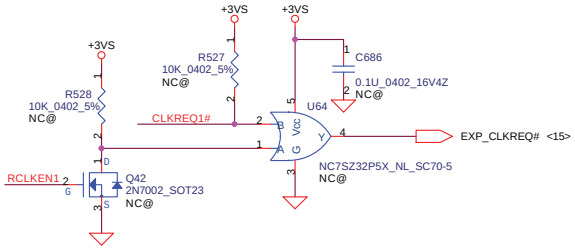
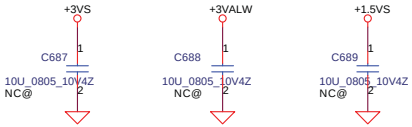
New Card Power Switch

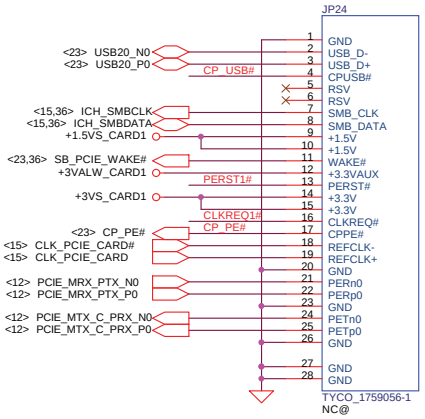








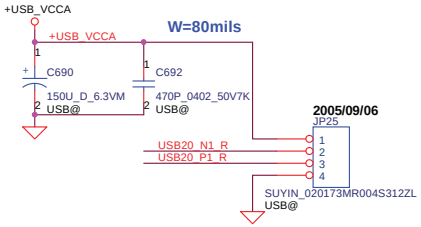
New Card Socket (Left)



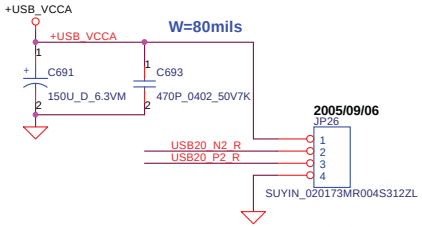
(NEW)

USB Component co-layout

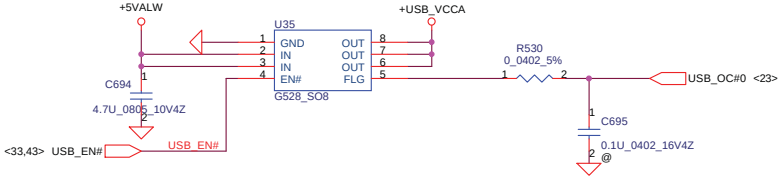
USB CONN. 1 & 2

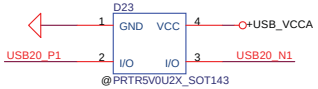


ECQ60



ECQ60





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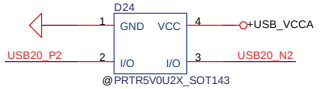

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Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

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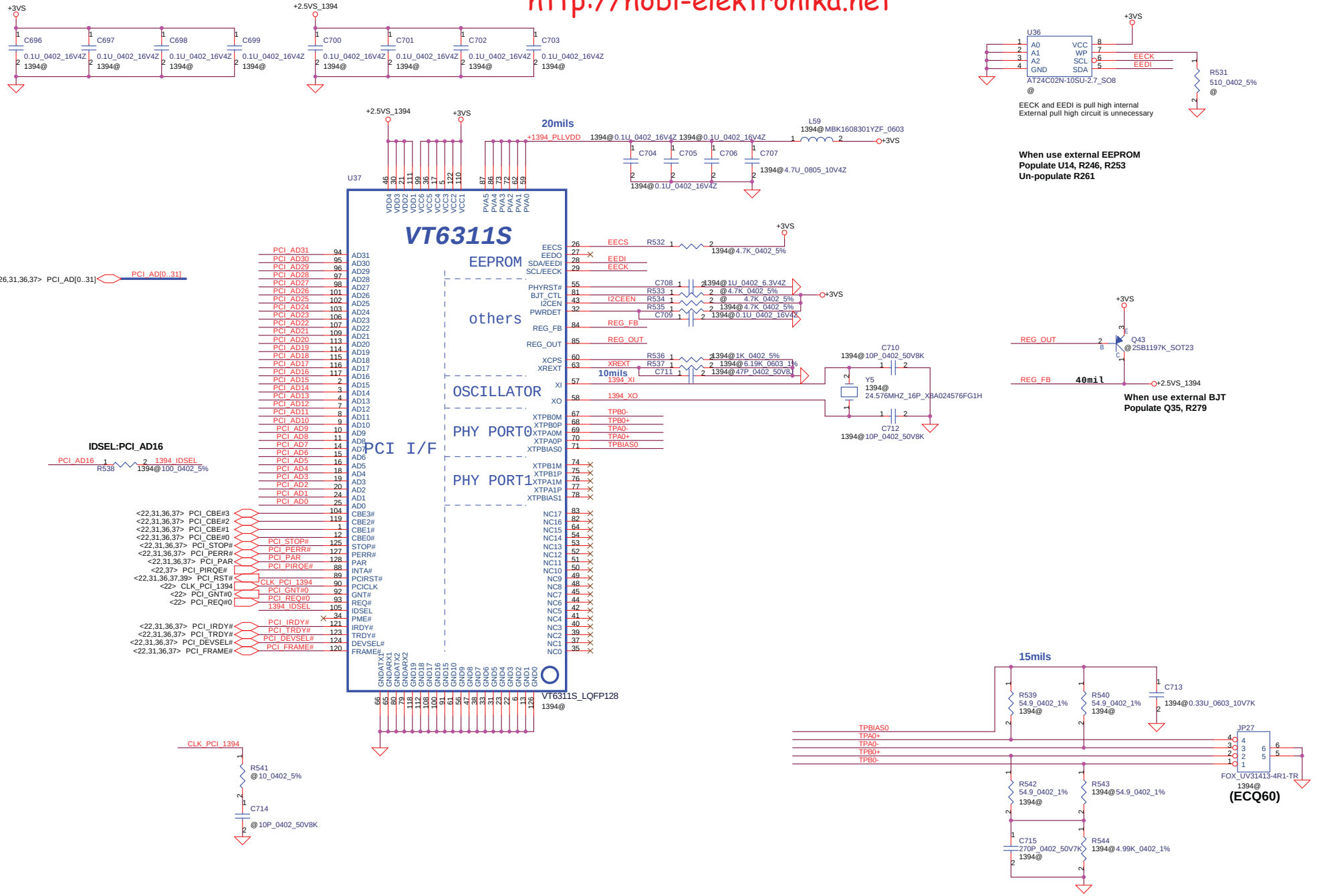

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Size	Document Number	Rev
Custom	401412	B

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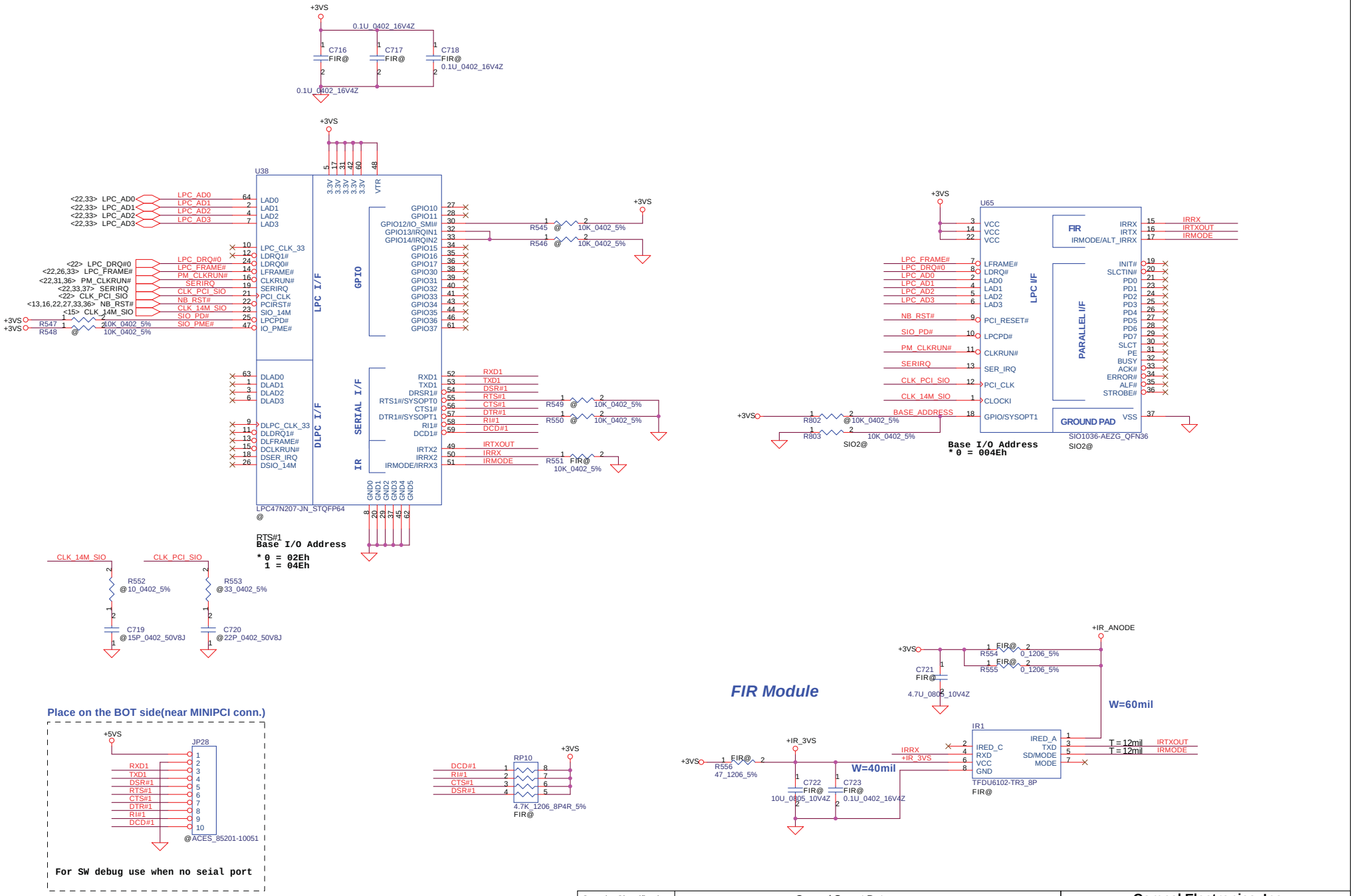

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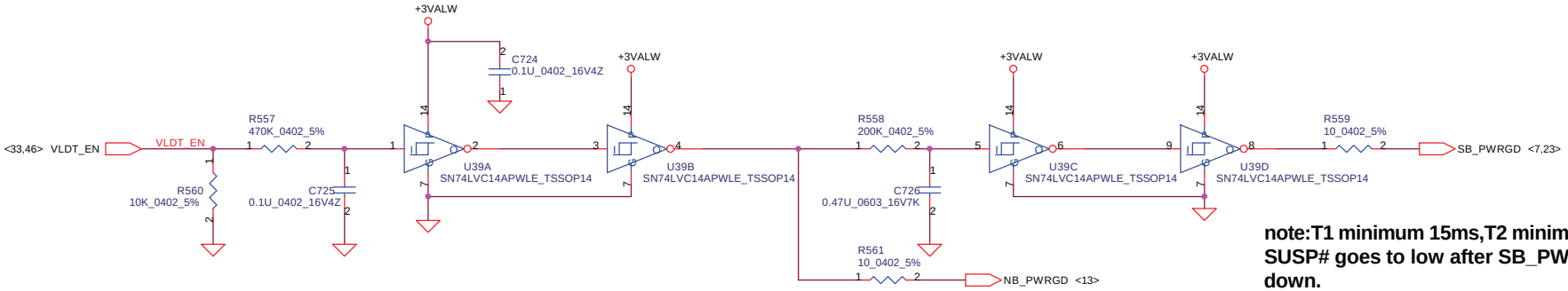
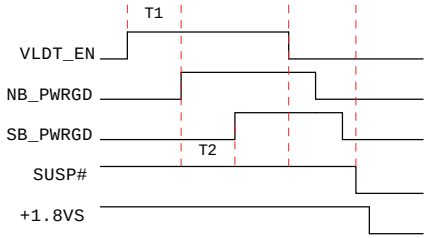
Power ON Circuit



note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



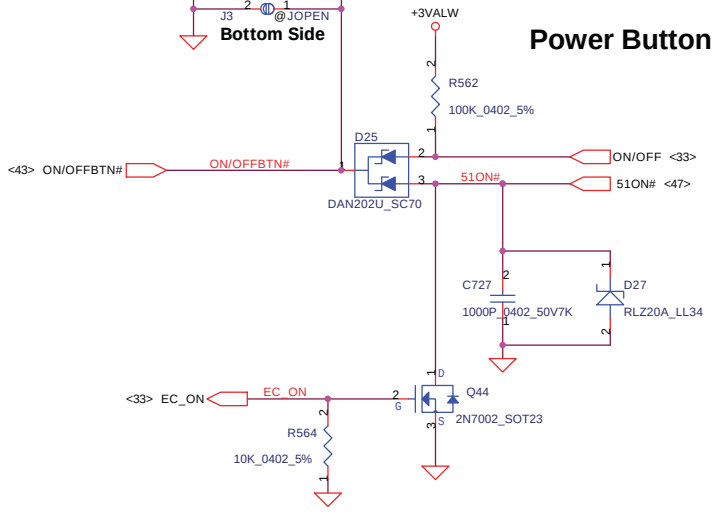
ON/OFF switch

TOP Side

J2 @JOPEN

J3 @JOPEN

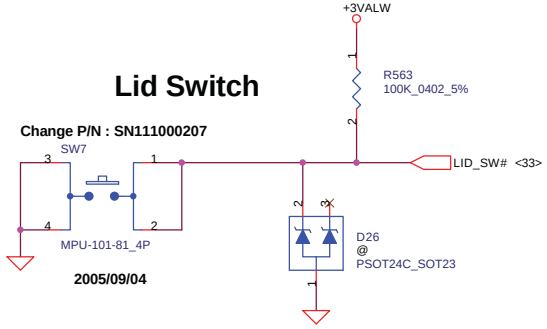
Bottom Side



Power Button

Lid Switch

Change P/N : SN111000207



2005/09/04

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

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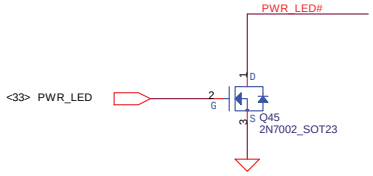
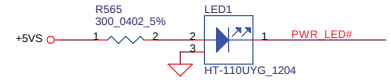
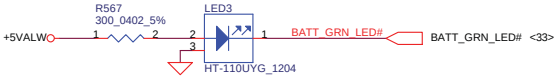
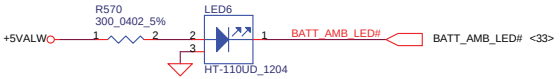
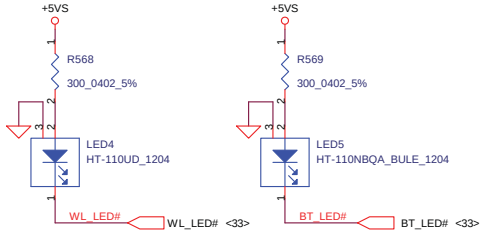
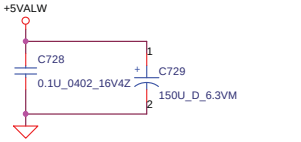




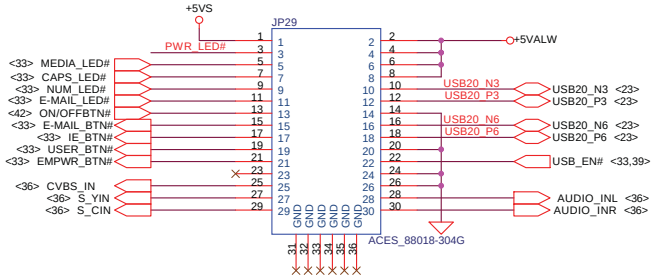




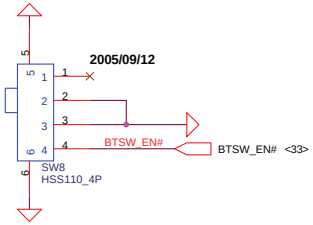




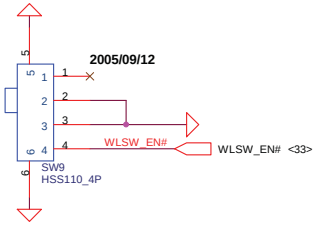
To LED/B Conn.

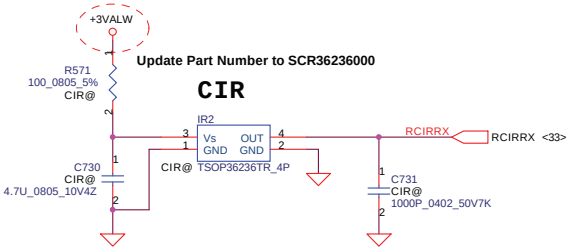


BT_SW



WL_SW





Geneva 2005/09/04 **Grapevine**

	KSO16	KSO17
KSI0	VOL_UP	LEFT
KSI1	RIGHT	VOL_DOWN
KSI2	PLAY	ENTER
KSI3	STOP	
KSI4	NEXT	
KSI5	REV	
KSI6		RECORD

	KSO16	KSO17
KSI2	PLAY	
KSI3	STOP	VOL_UP
KSI4	NEXT	VOL_DOWN
KSI5	REV	ARCADE_TV

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Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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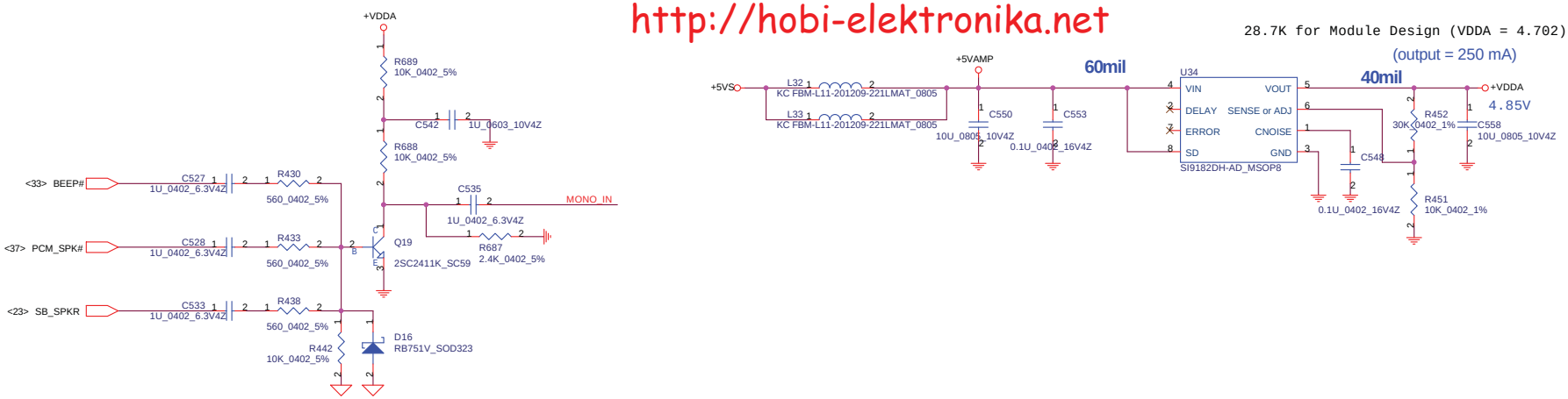
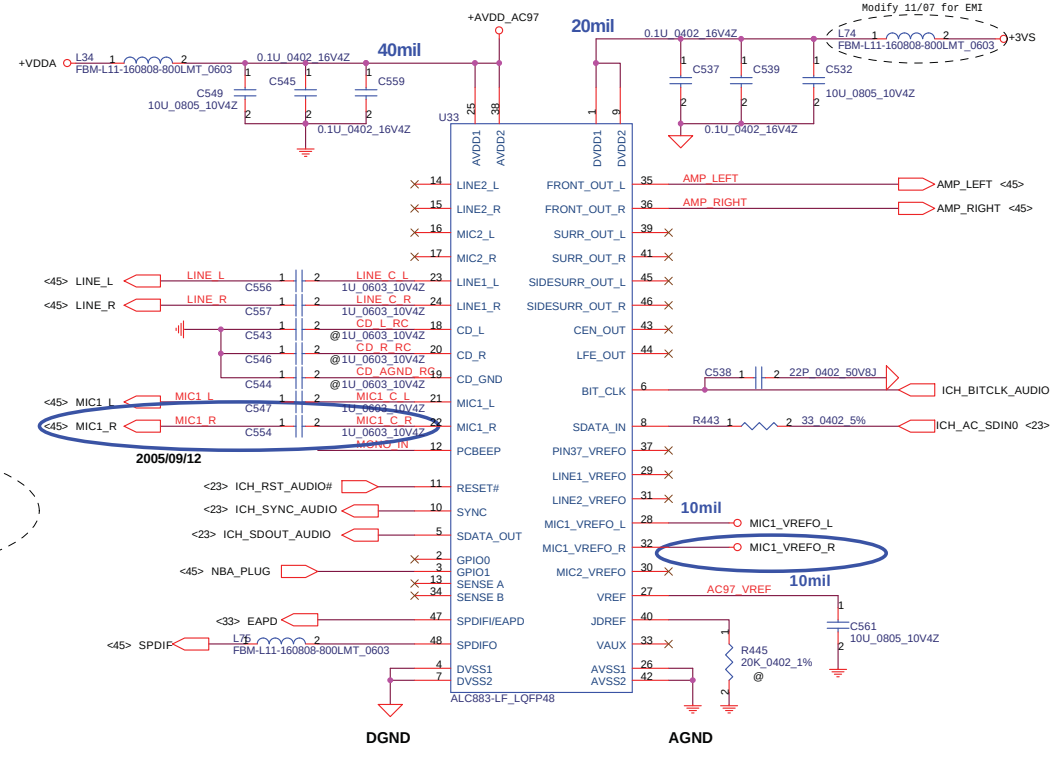
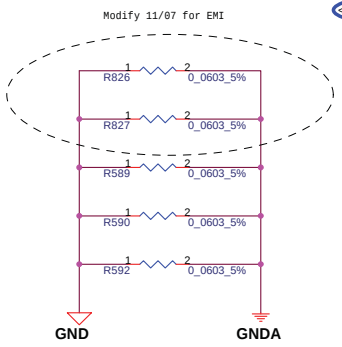
28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)



HD Audio Codec





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Compal Electronics, Inc.

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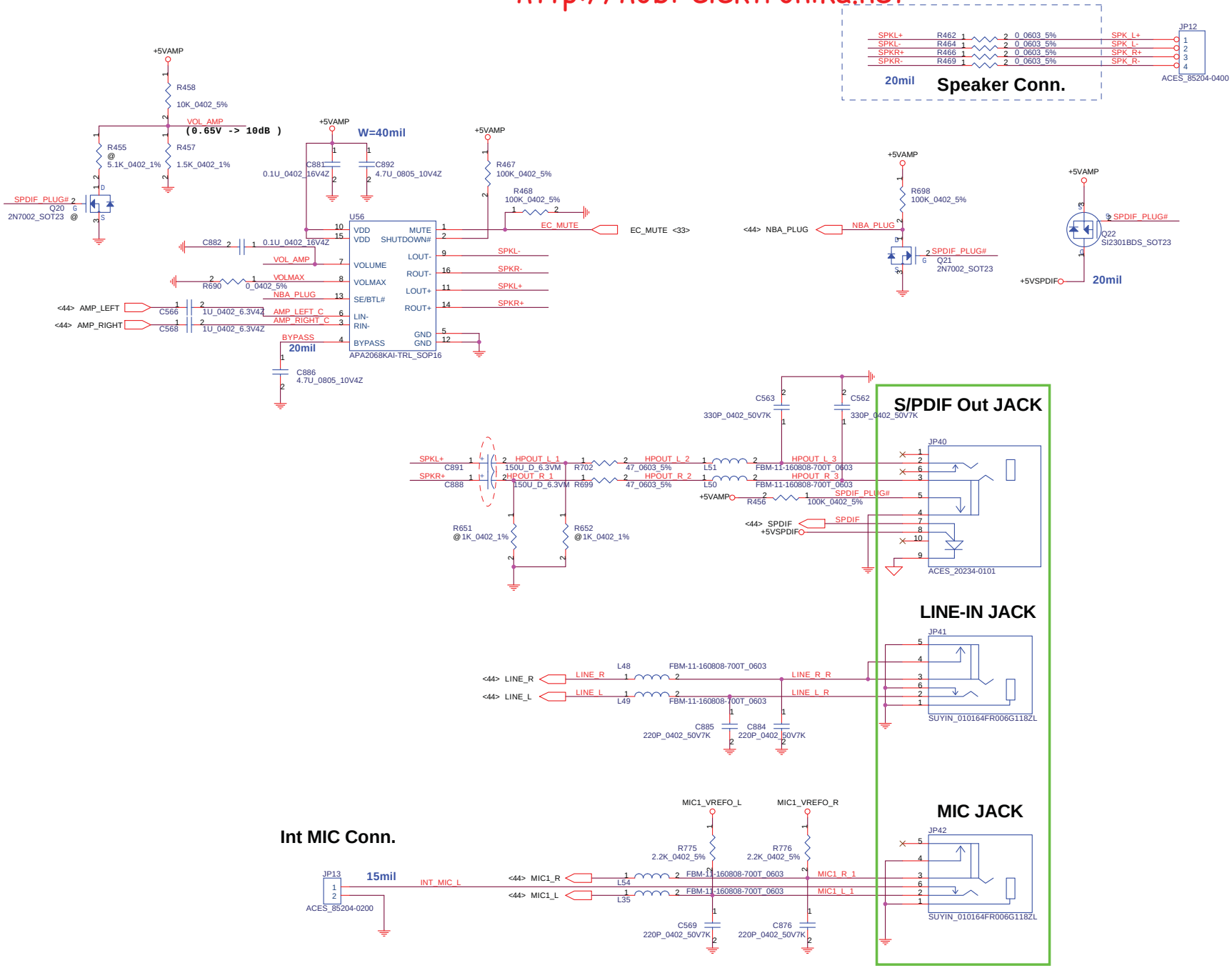

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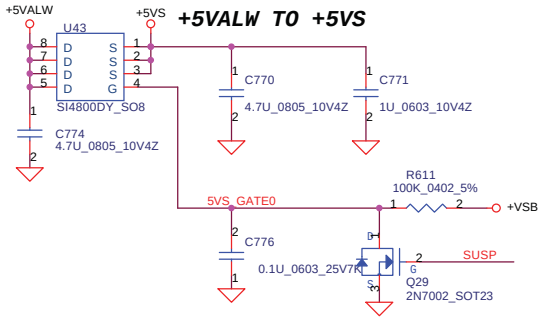
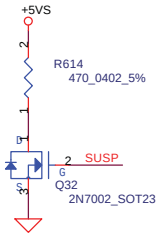
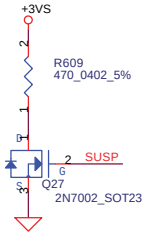
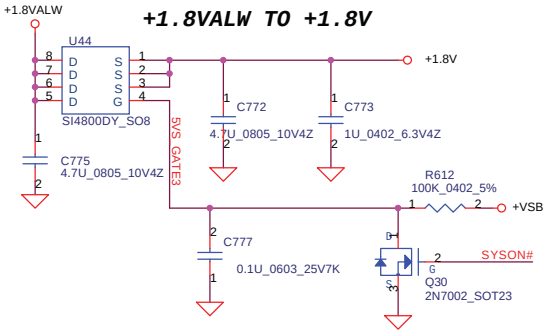
+5VALW TO +5VS

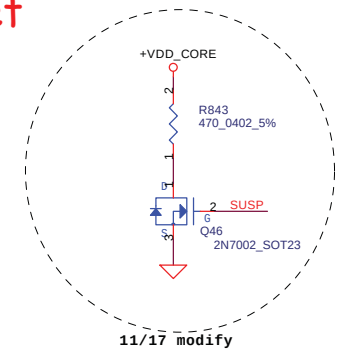


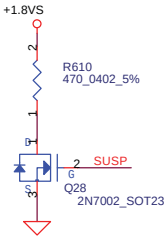


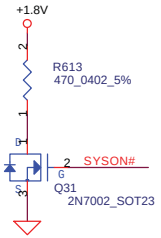


+1.8VALW TO +1.8V

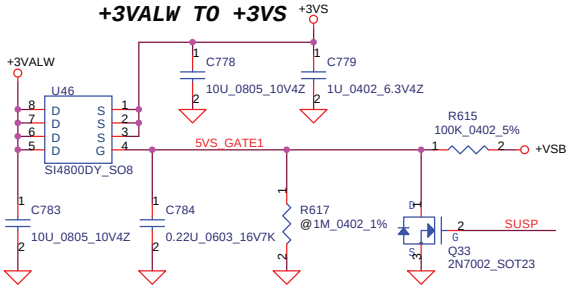




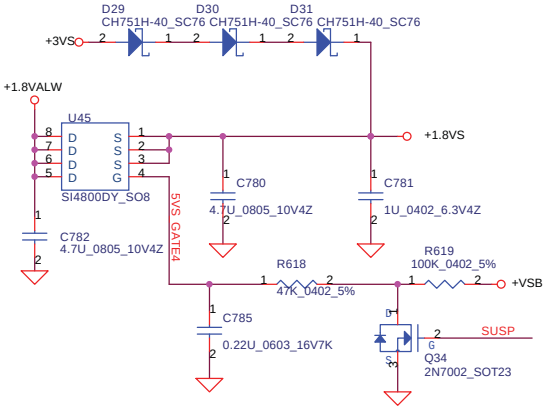


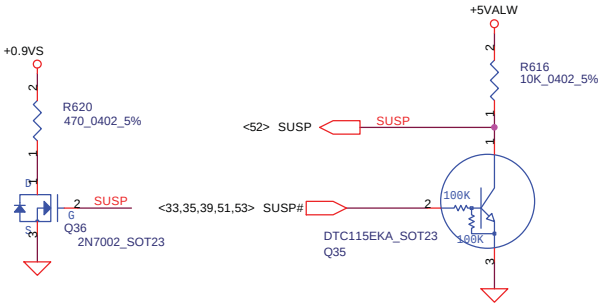


+3VALW TO +3VS

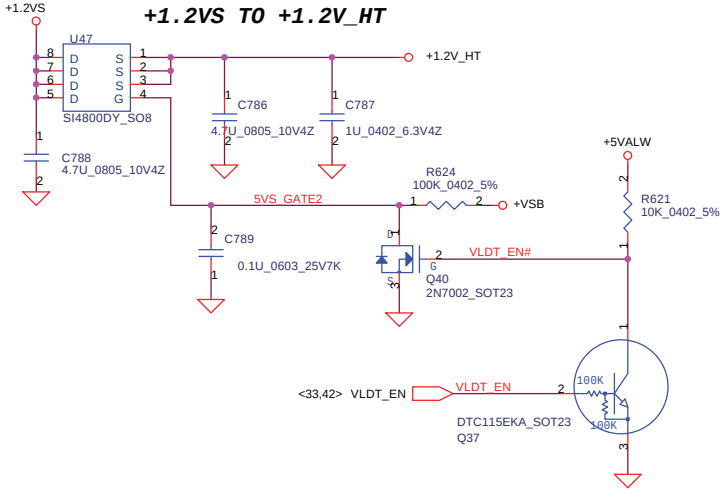


+1.8VALW TO +1.8VS

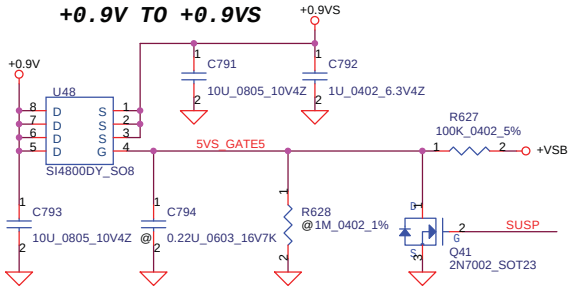


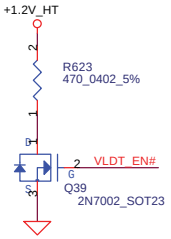


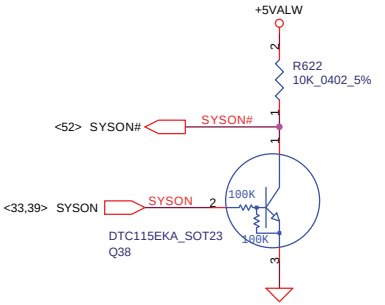
+1.2VS TO +1.2V_HT



+0.9V TO +0.9VS







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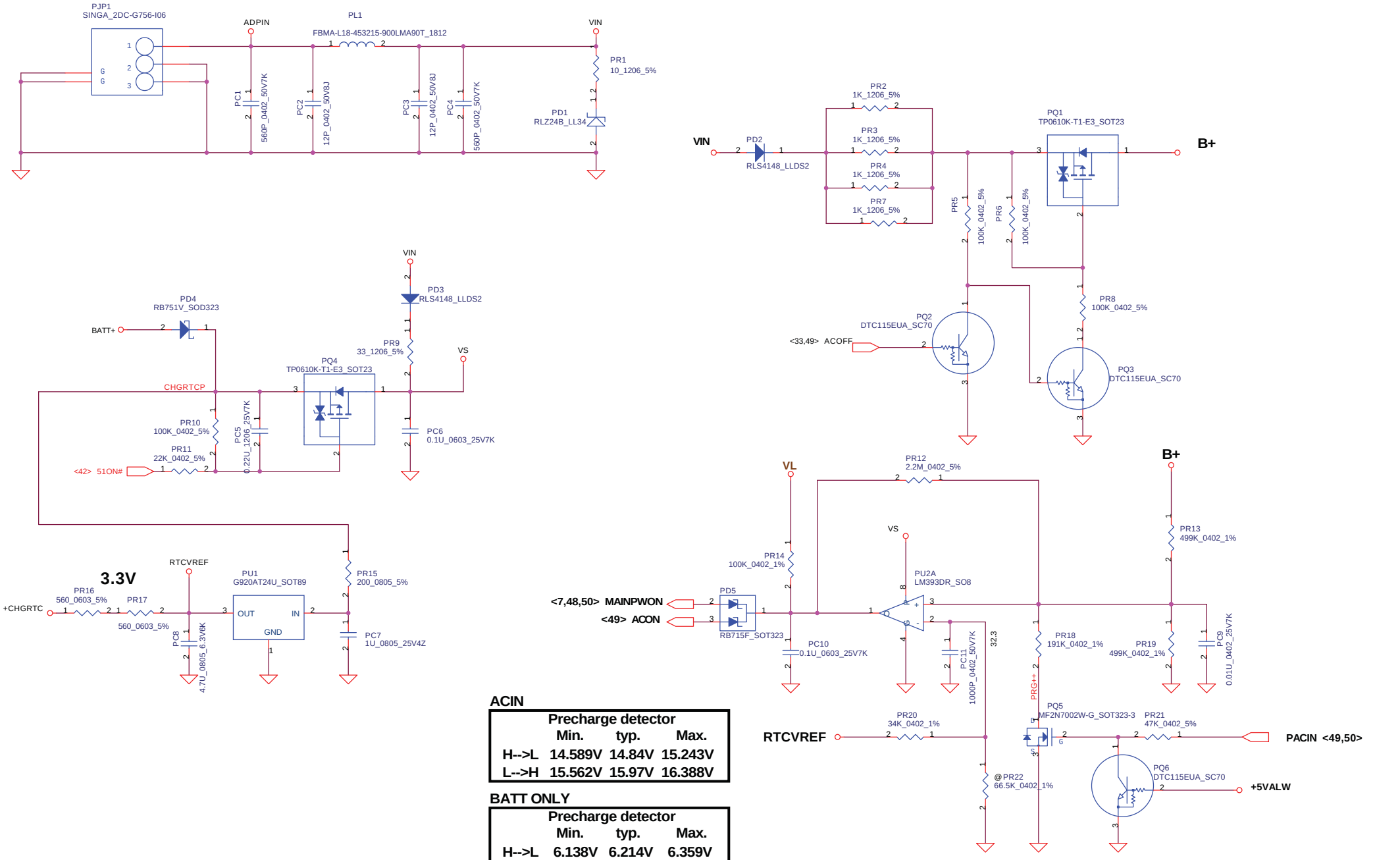

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2005/0926	Deciphered Date	2006/0926

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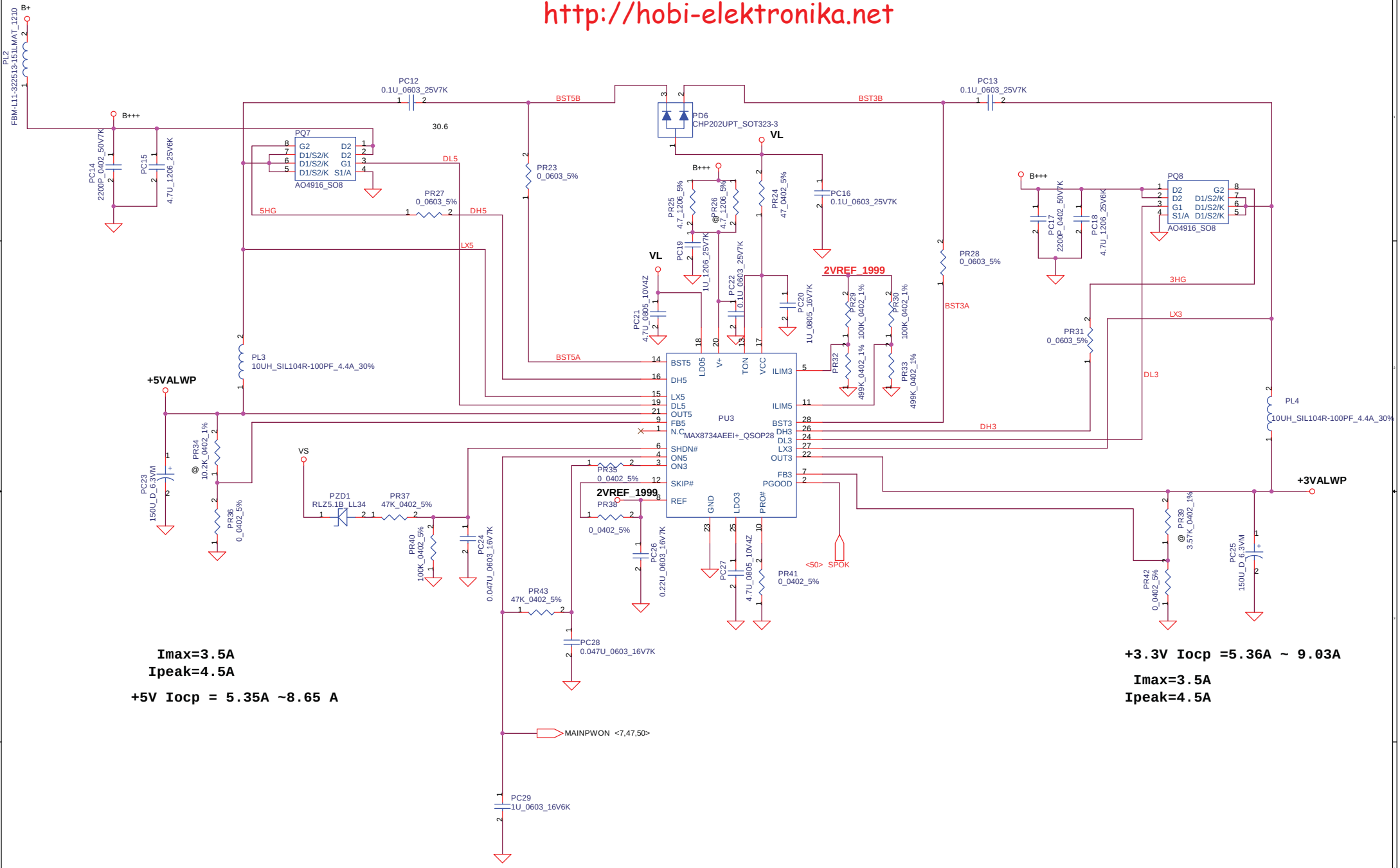

Imax=3.5A
Ipeak=4.5A

+5V Iocp = 5.35A ~8.65 A

+3.3V Iocp =5.36A ~ 9.03A

Imax=3.5A
Ipeak=4.5A

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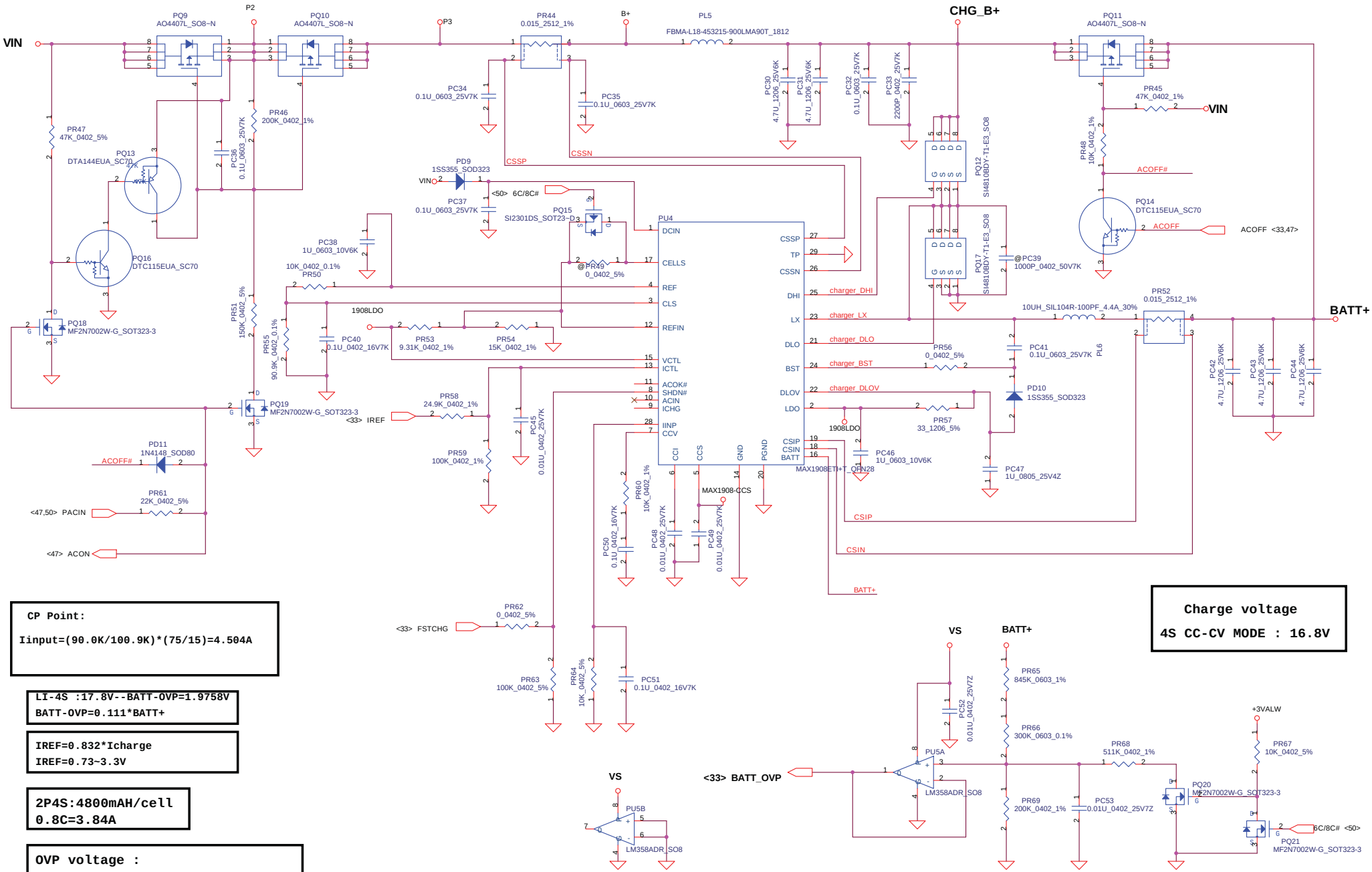
Charger

Iadp=0~4.5A(90W)



CP Point:

Iinput=(90.0K/100.9K)*(75/15)=4.504A

LI-4S :17.8V--BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

IREF=0.832*Icharge
IREF=0.73~3.3V

2P4S:4800mAH/cell
0.8C=3.84A

OVP voltage :
LI-3S :17.8V----BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

Charge voltage
4S CC-CV MODE : 16.8V

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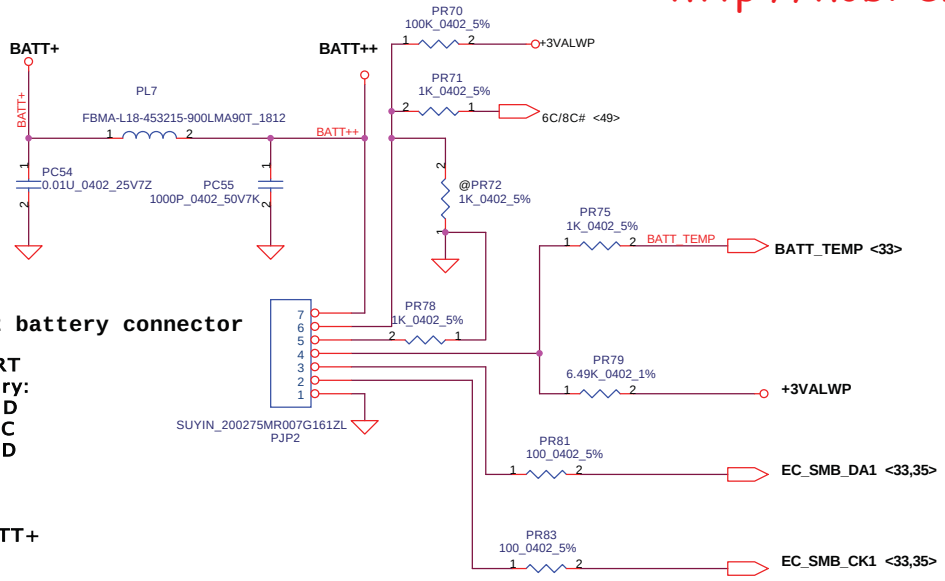
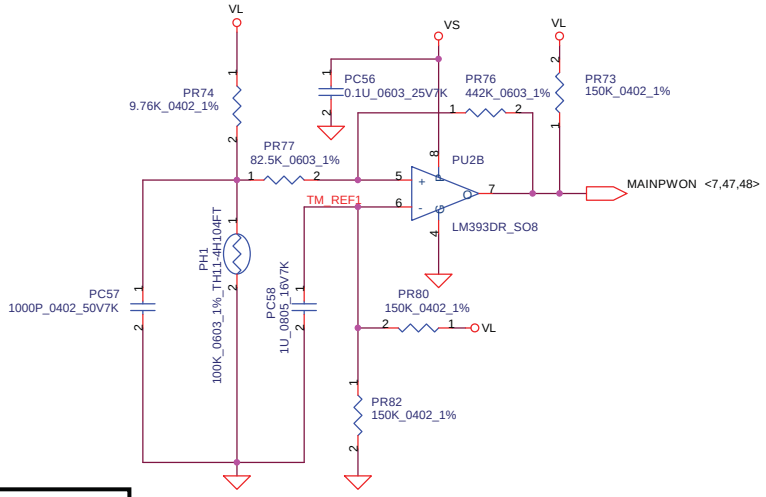
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C

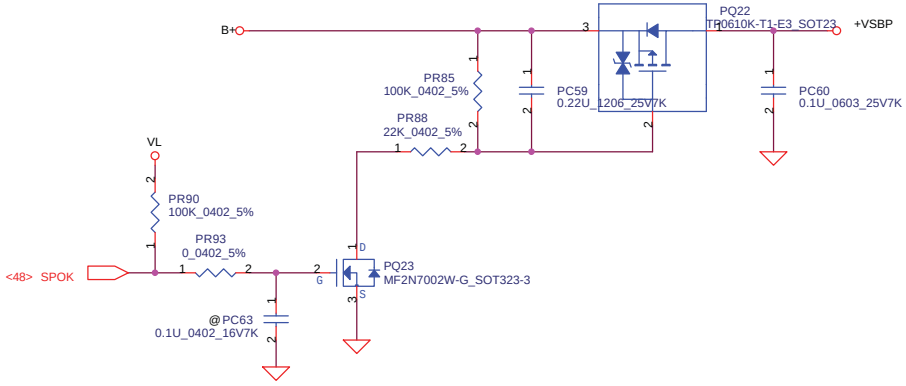
PJP2 battery connector

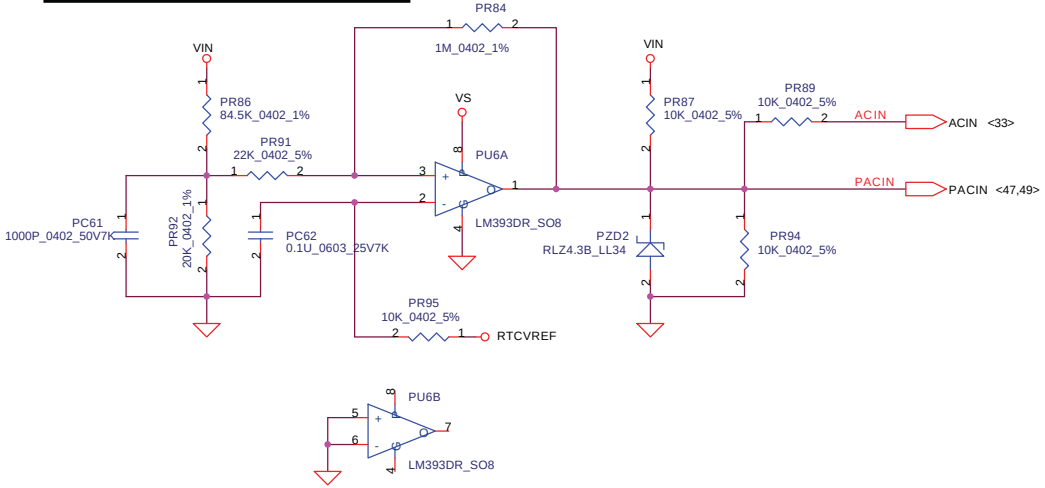
SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+





Vin Detector	Min.	typ.	Max.
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V





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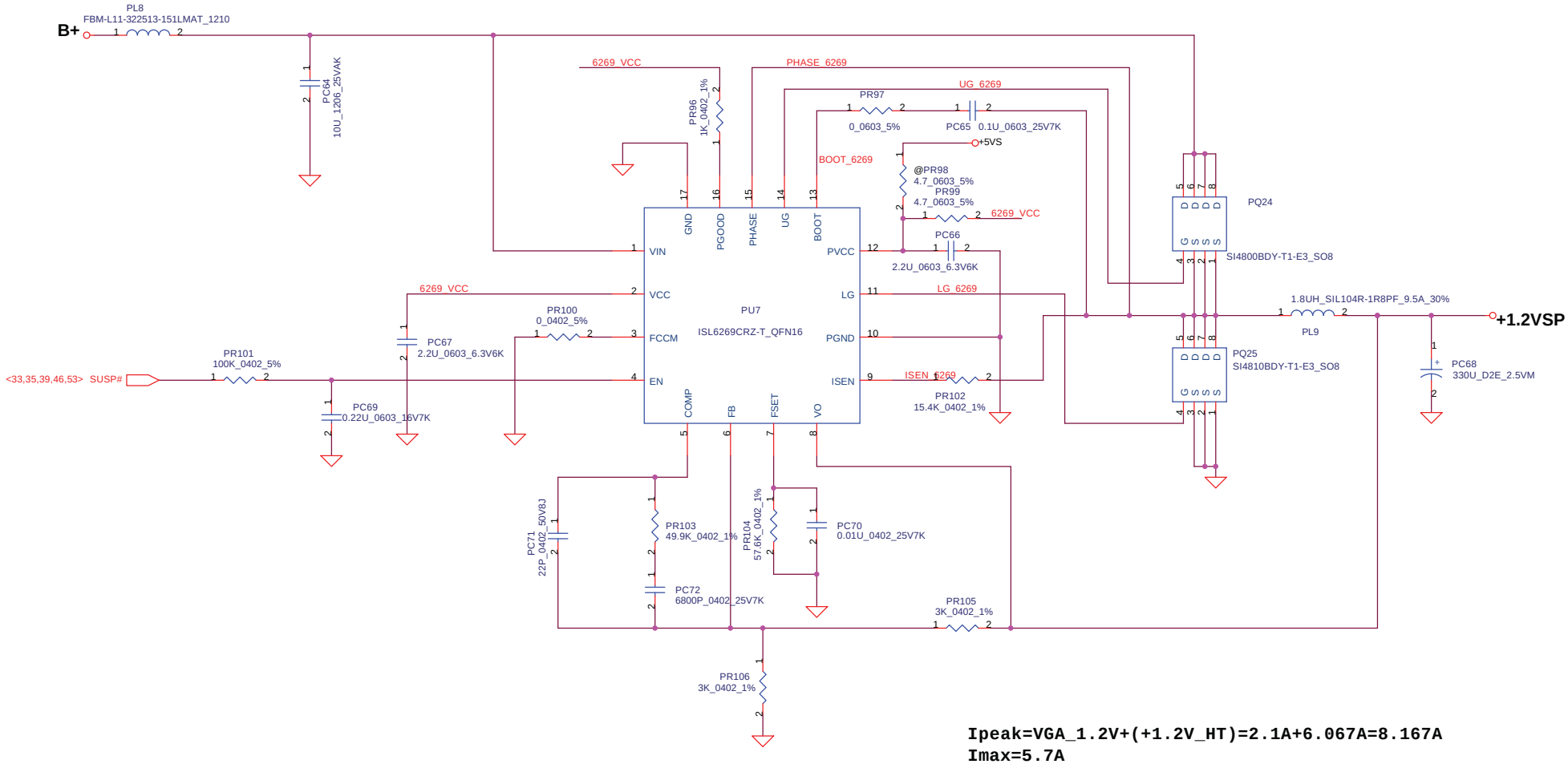

Ipeak=VGA_1.2V+(+1.2V_HT)=2.1A+6.067A=8.167A
Imax=5.7A
Iocmin=9.23A
Iocmax=19.23A

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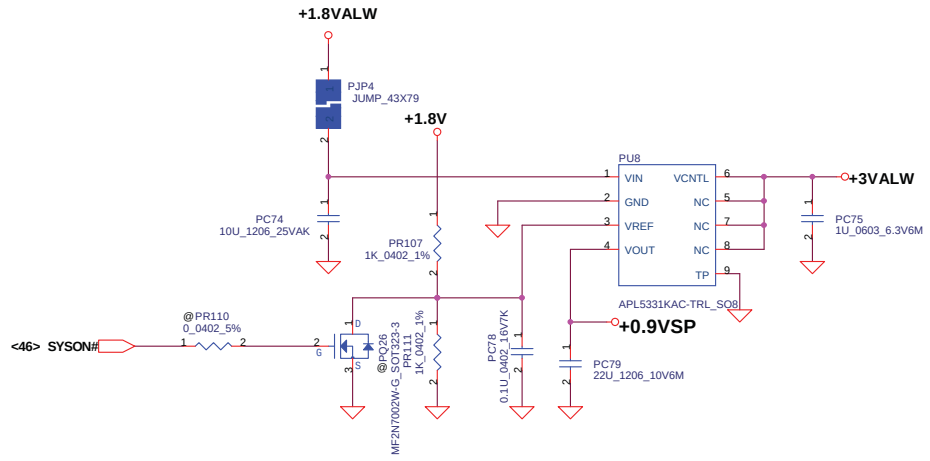

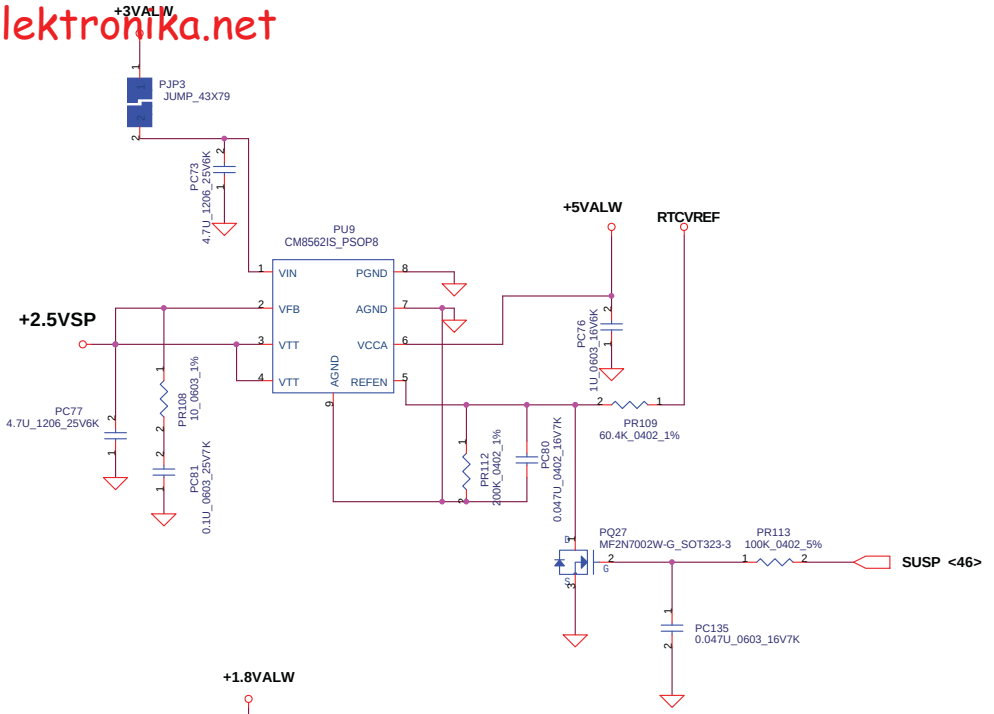

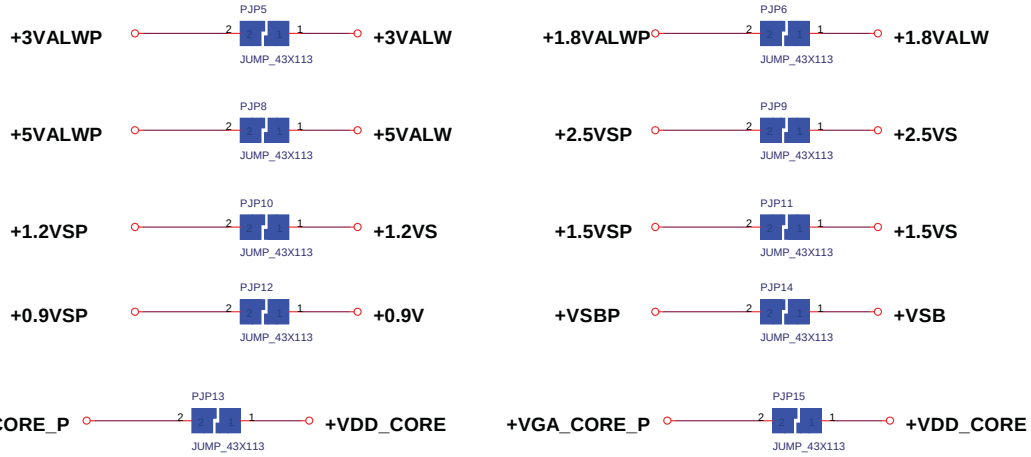

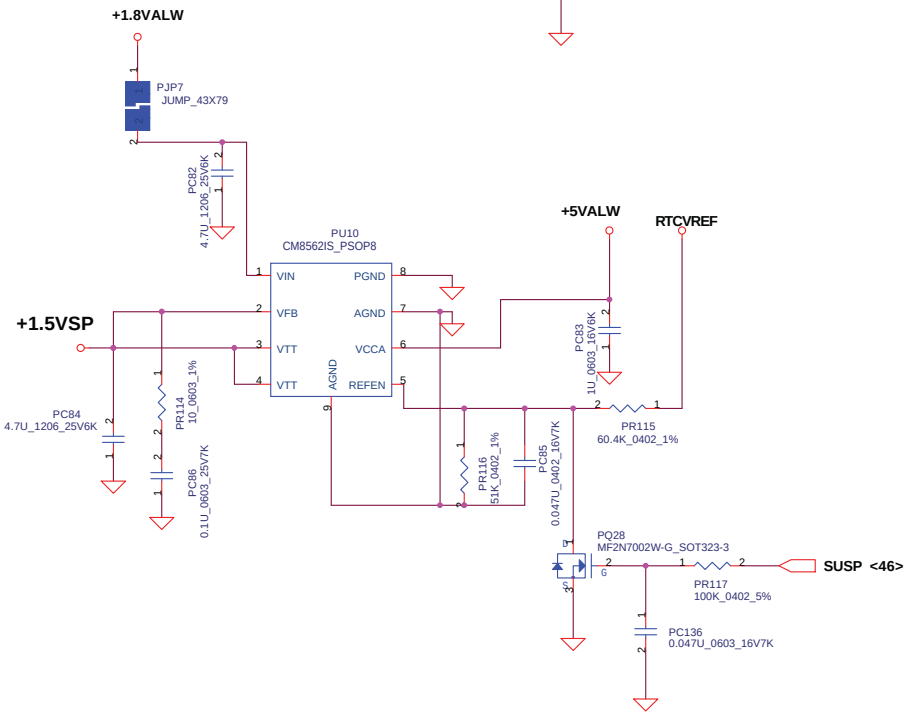

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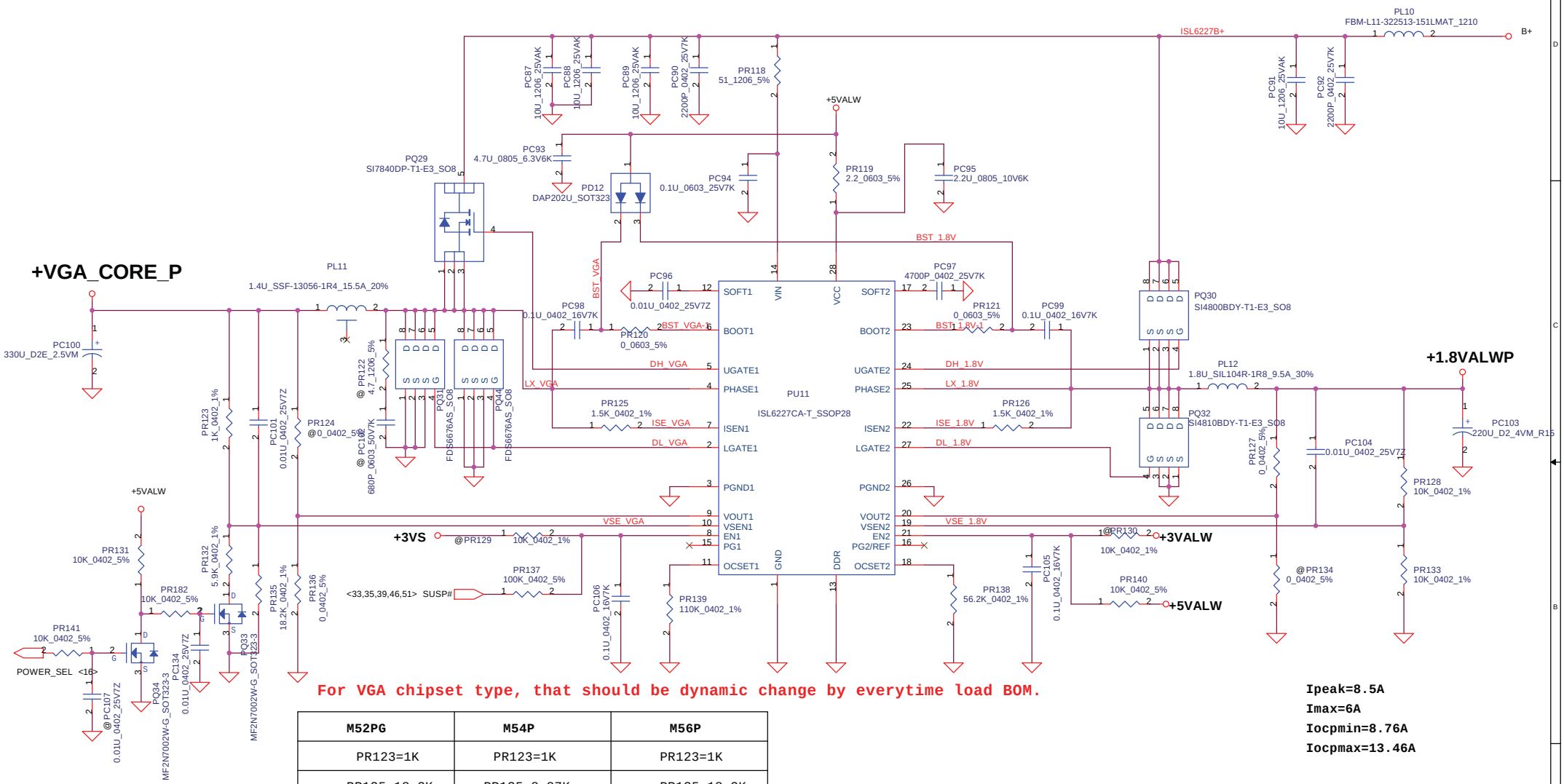

For VGA chipset type, that should be dynamic change by everytime load BOM.

M52PG	M54P	M56P
PR123=1K	PR123=1K	PR123=1K
PR135=18.2K	PR135=8.87K	PR135=18.2K
PR132=17.8K	PR132=8.87K	PR132=5.9K
L=1.000V	**L=1.102V**	**L=1.102V**
H=0.949V	**H=1.001V**	**H=0.949V**

Ipeak=16.40A
Imax=12.25A
Iocpmin=22.07A
Iocpmax=38.67A

Ipeak=8.5A
Imax=6A
Iocpmin=8.76A
Iocpmax=13.46A

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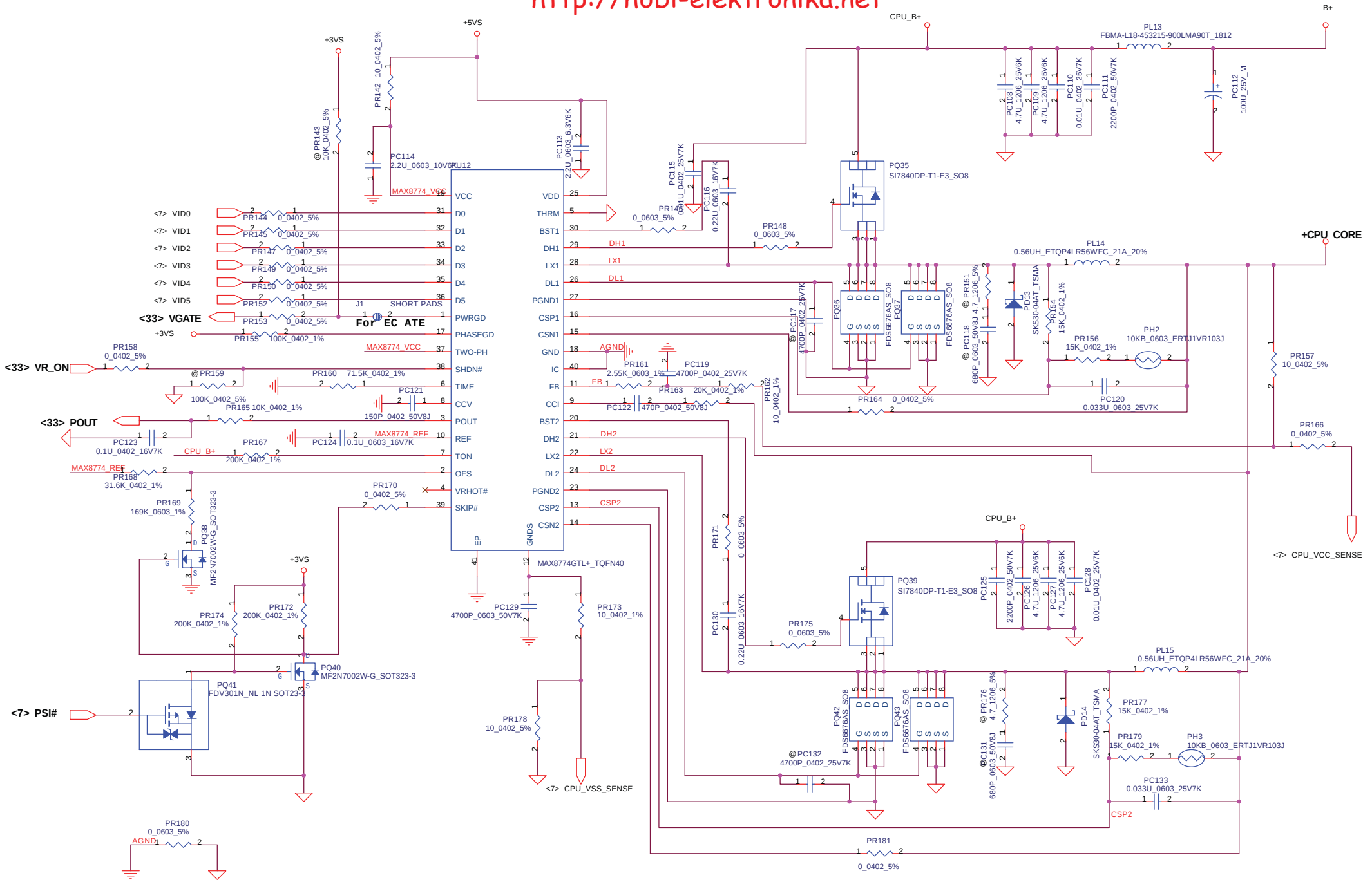

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
8							
9							

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